

FIG.2

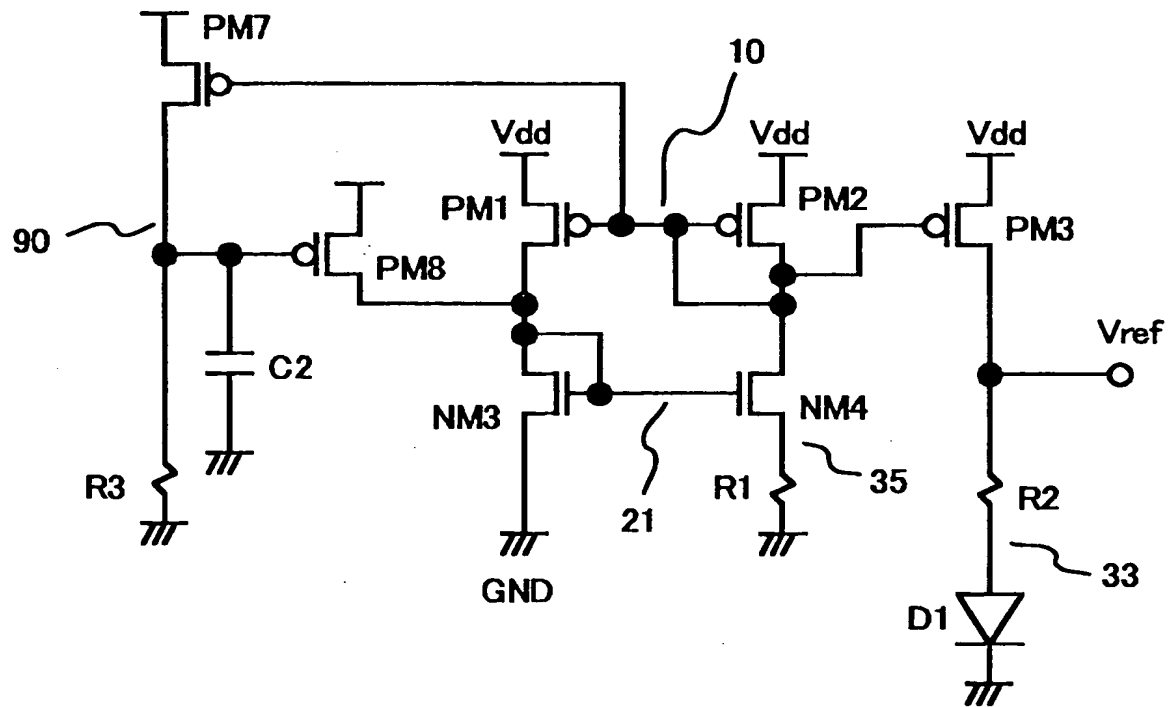


FIG.3

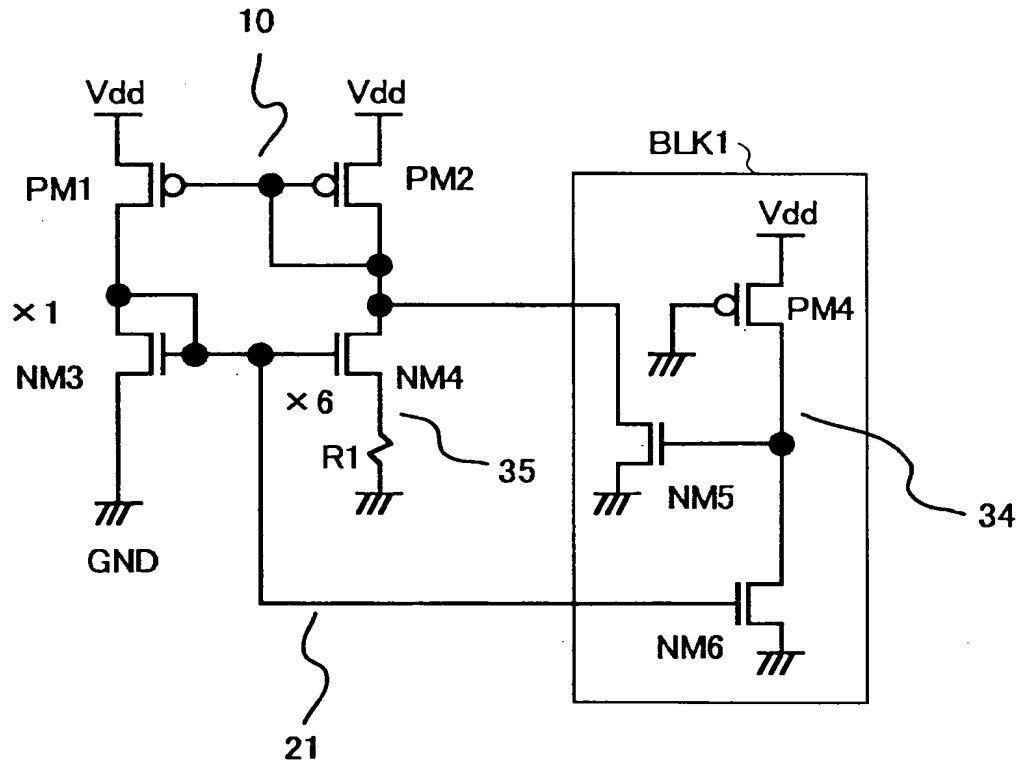
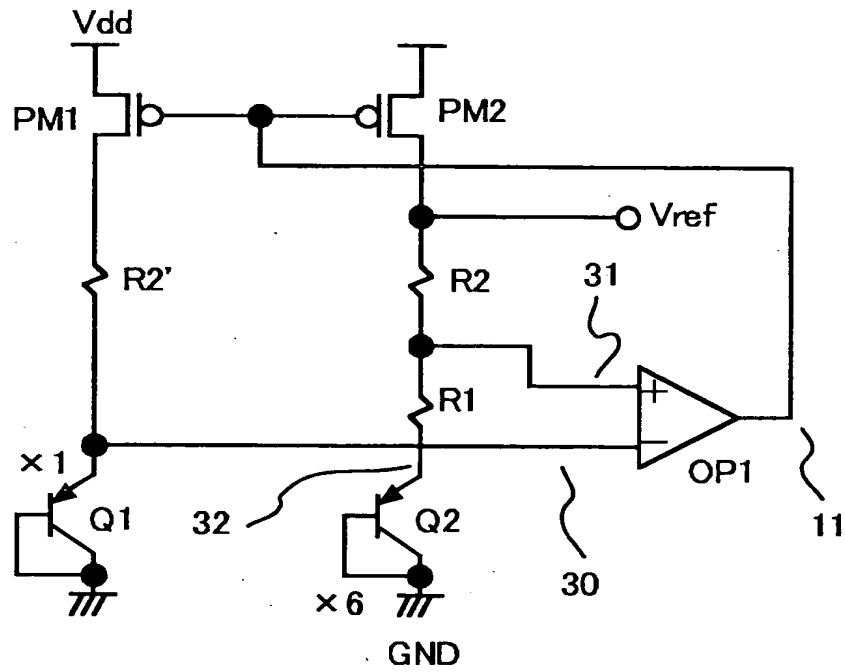


FIG.4



### FIG.5

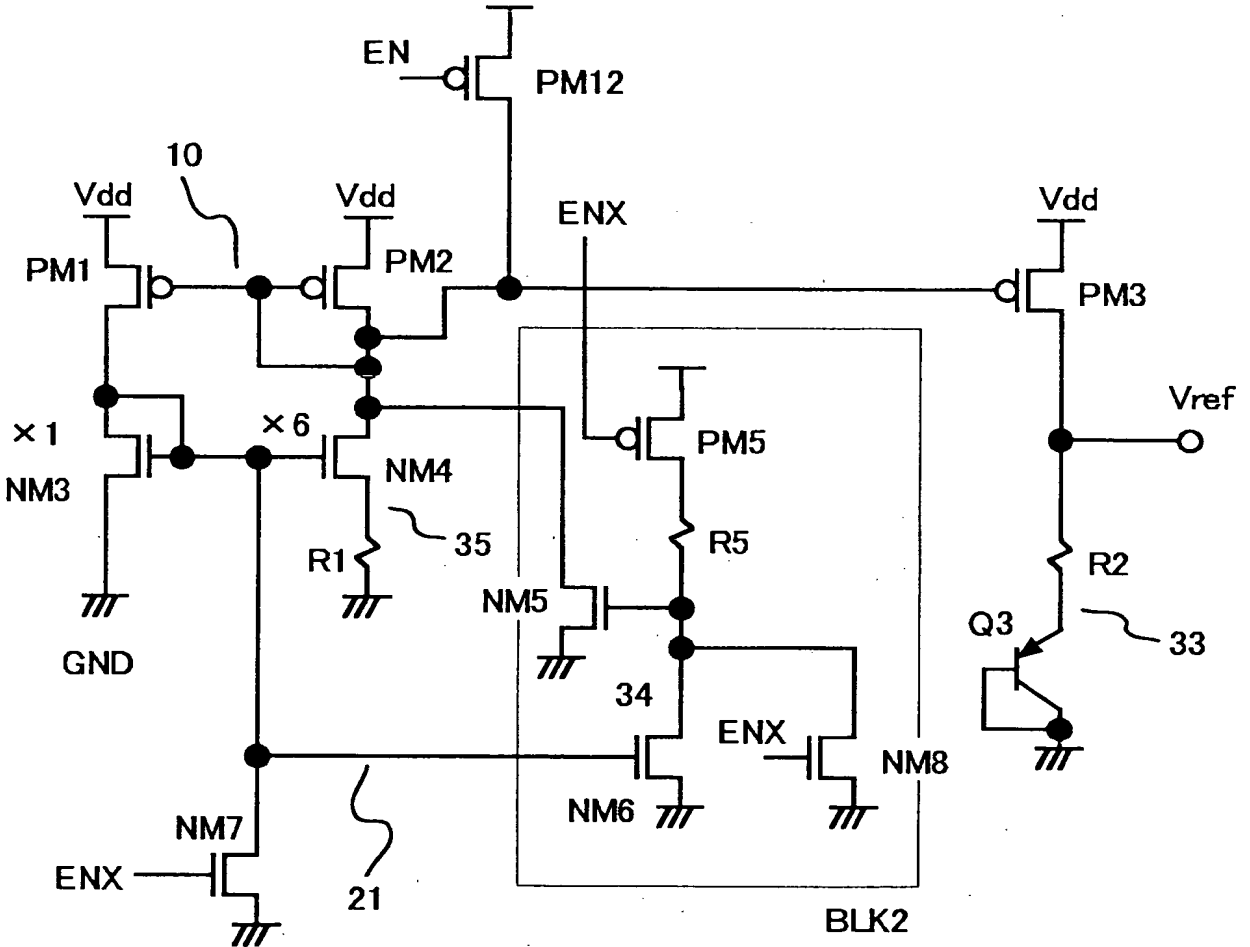


FIG.6

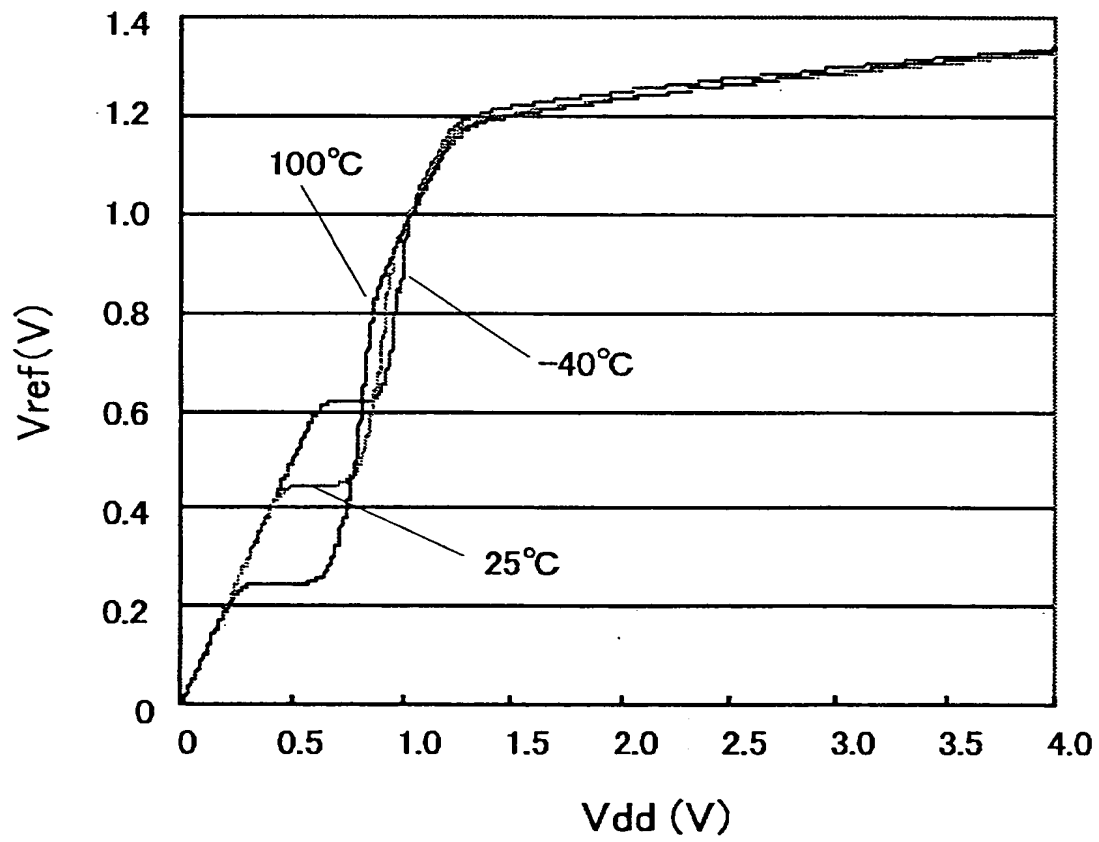
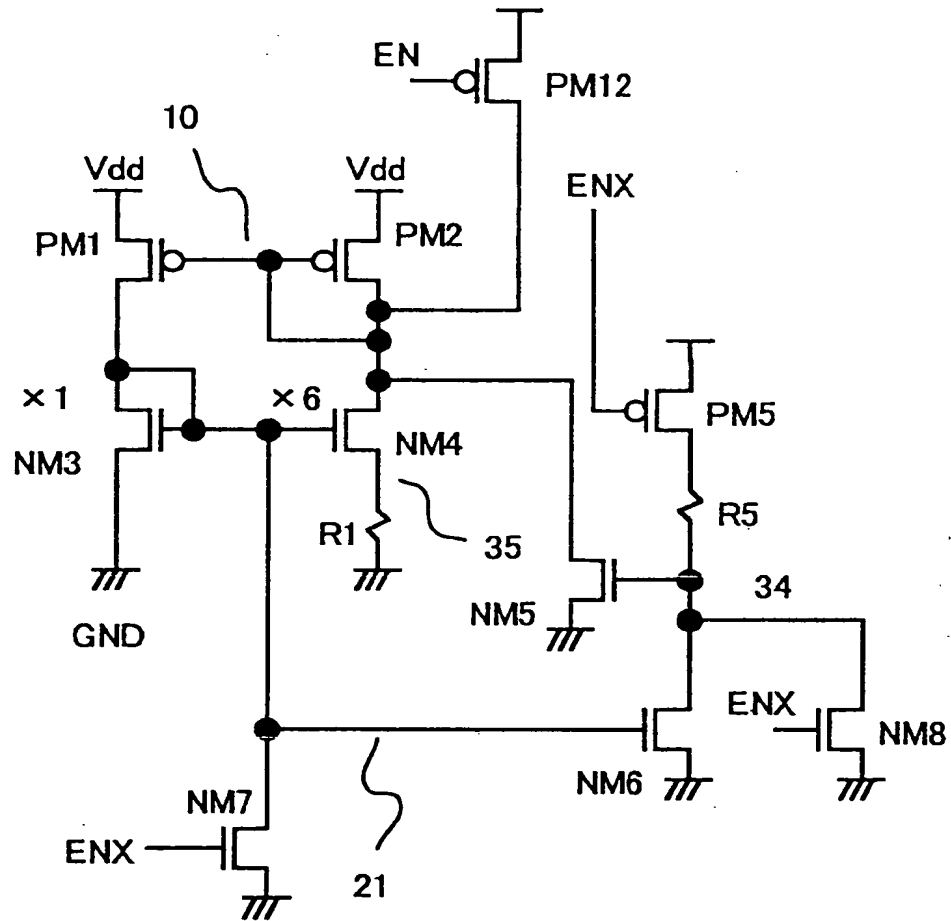


FIG. 7



**FIG. 8**

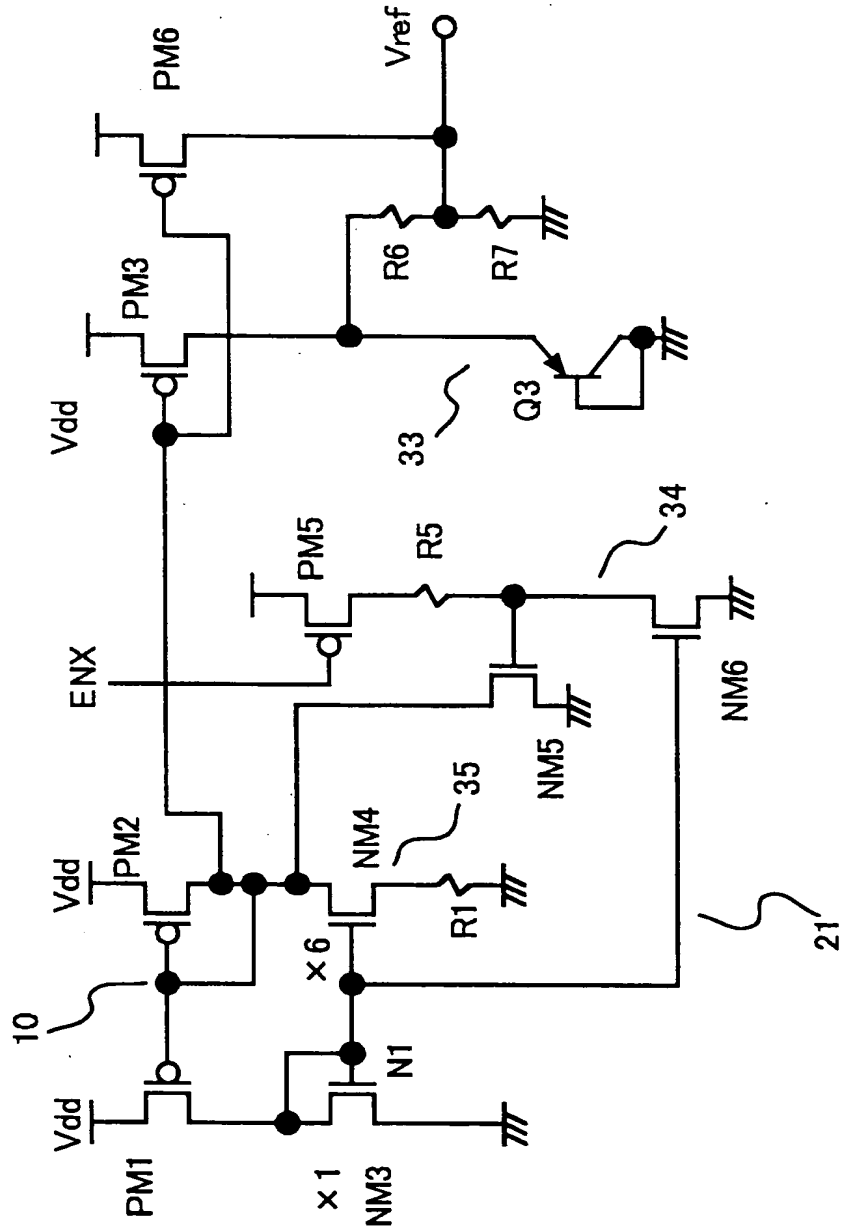




FIG.9

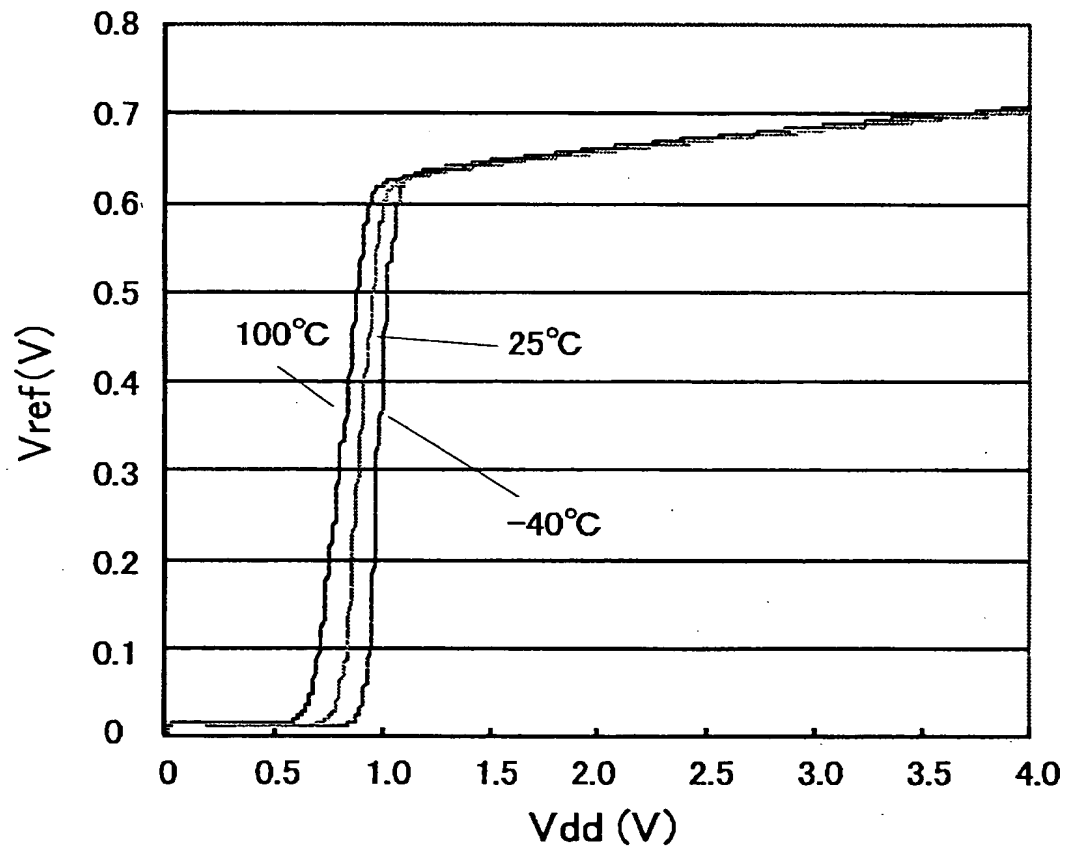


FIG.10

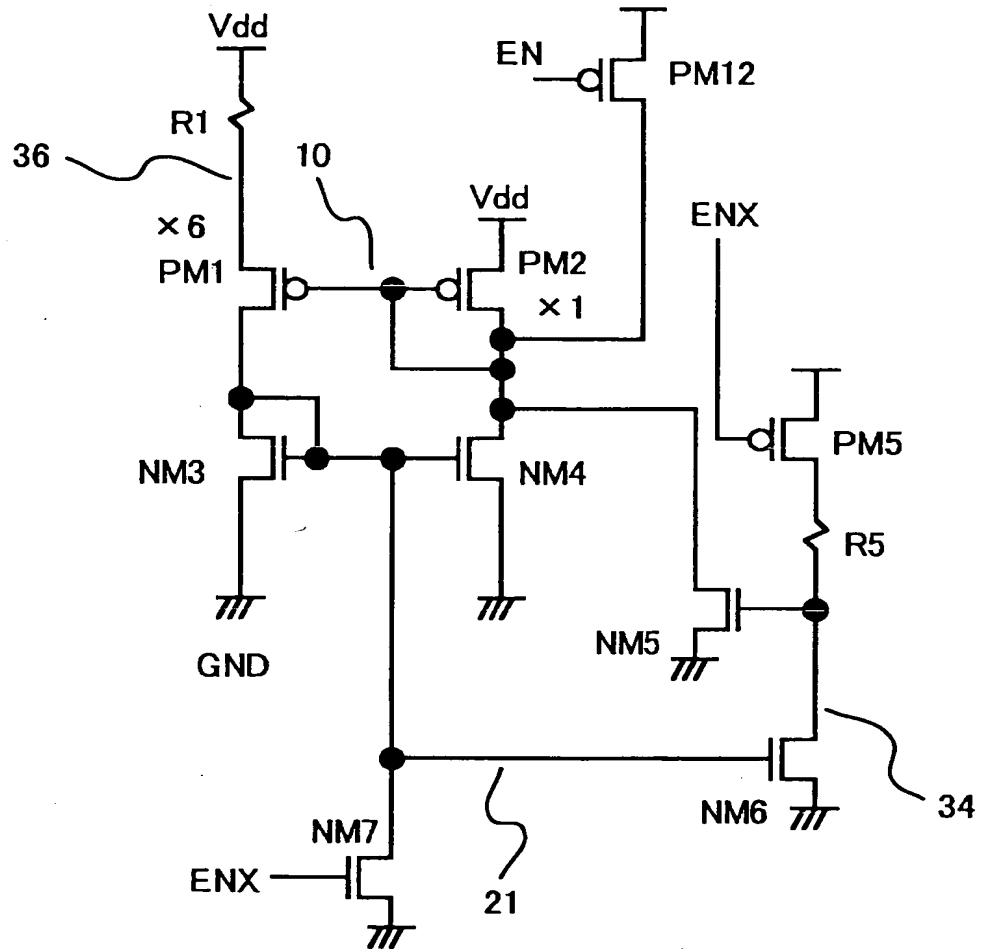


FIG.11

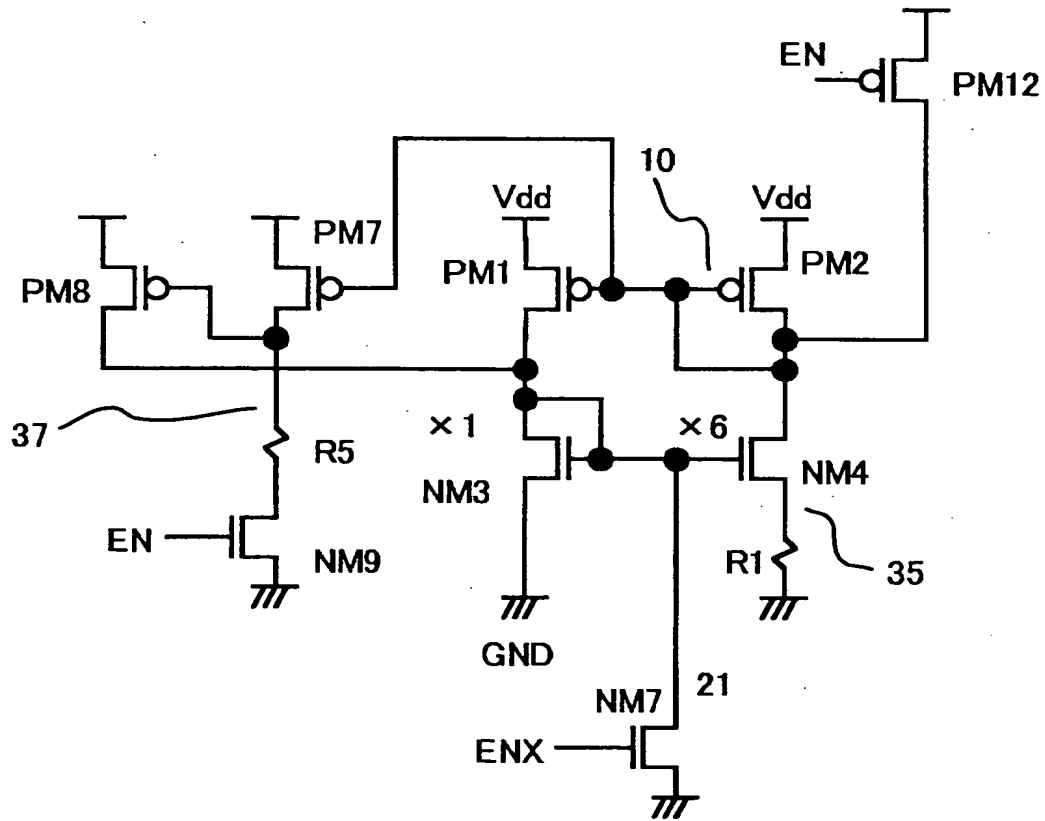


FIG.12

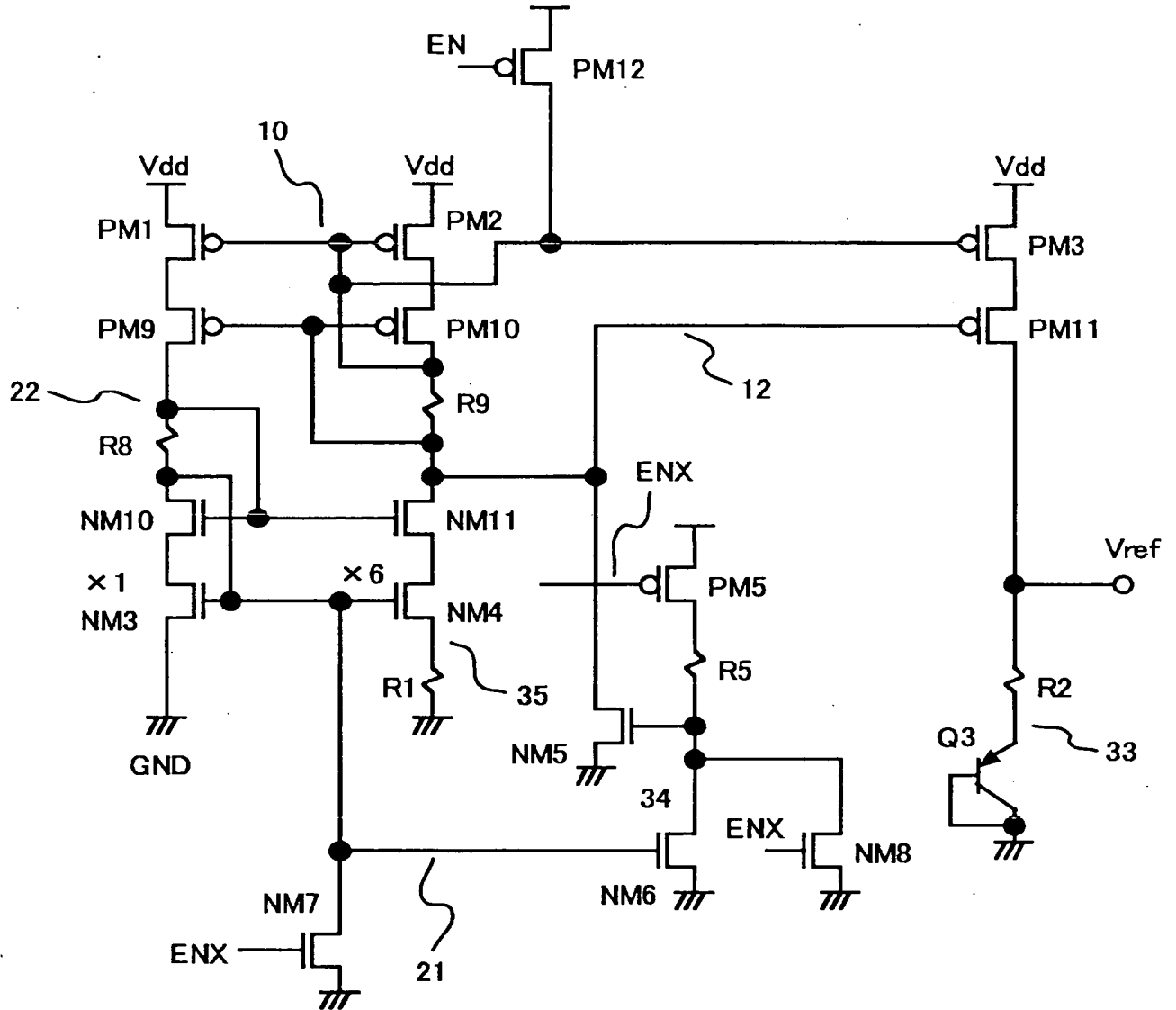
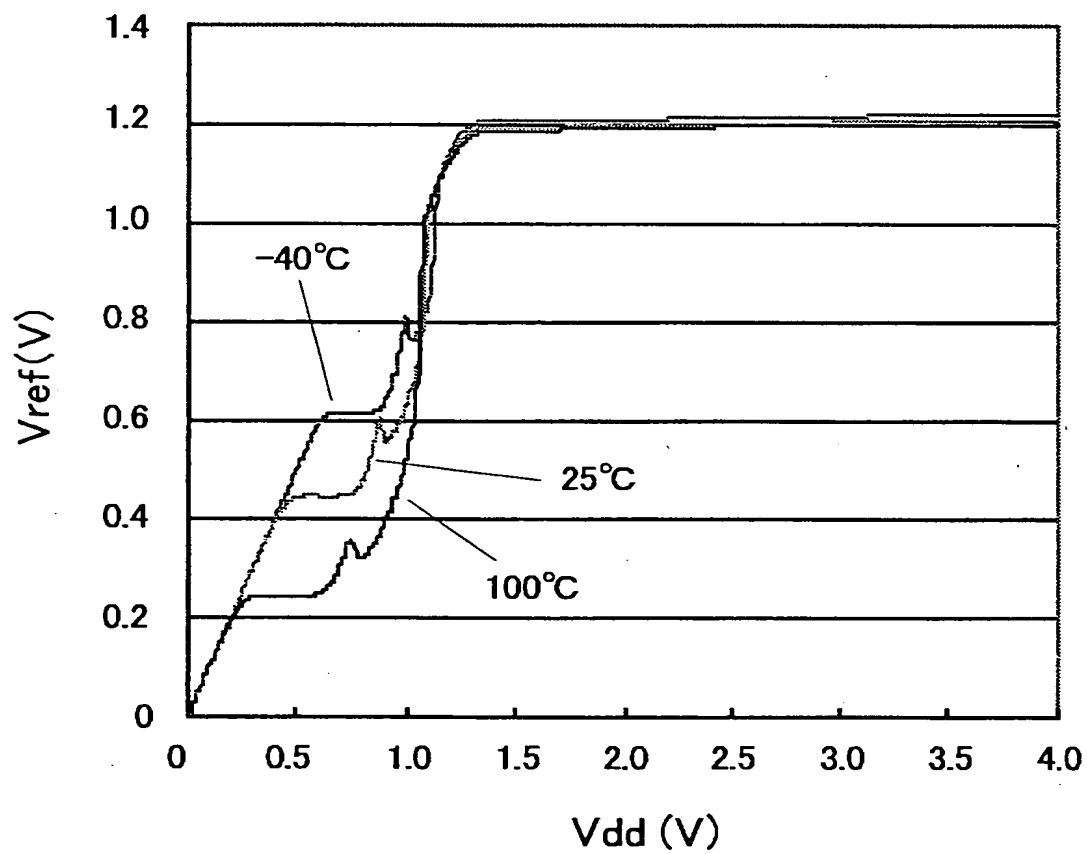


FIG.13



**FIG. 14**

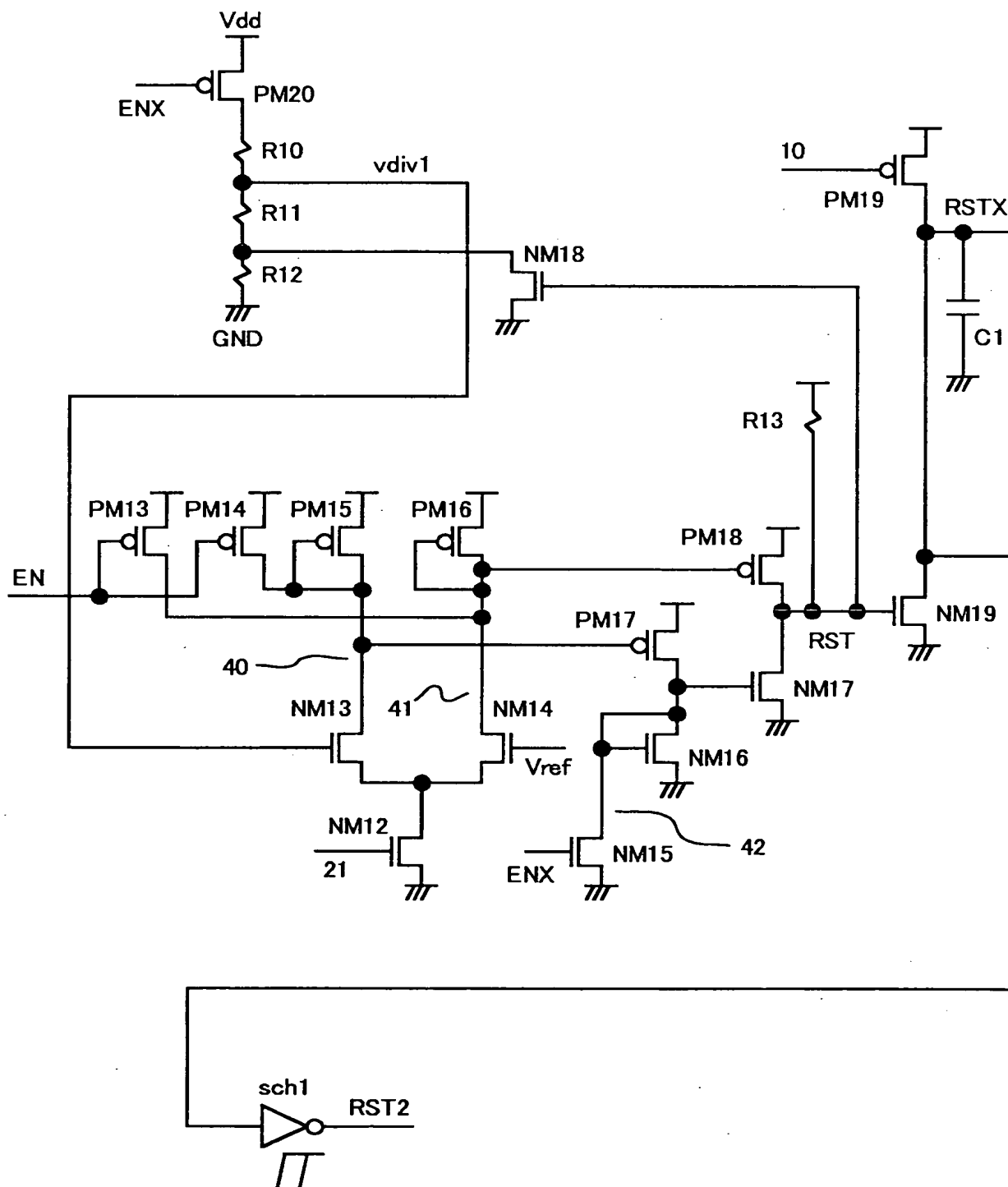


FIG.15

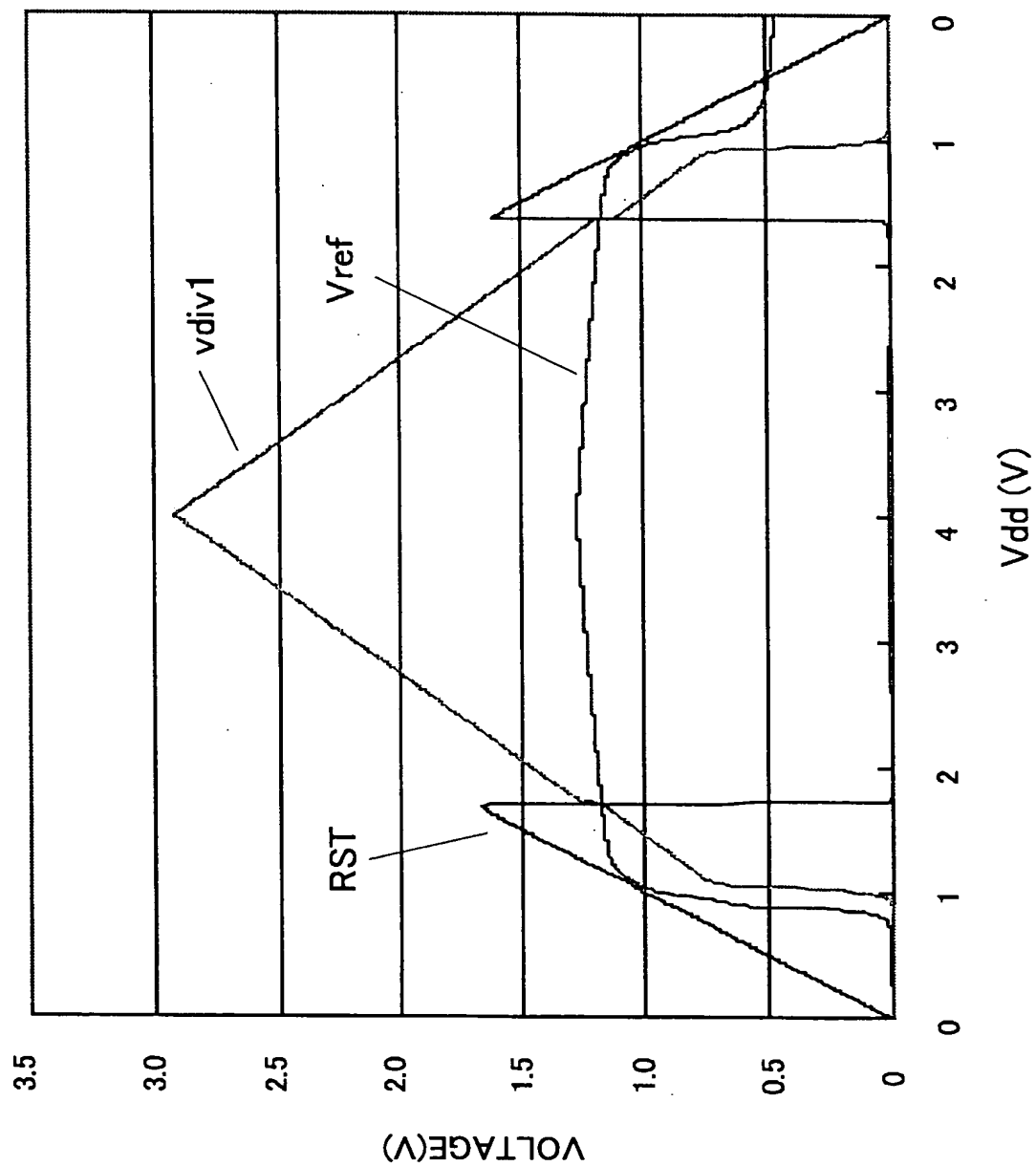


FIG.16

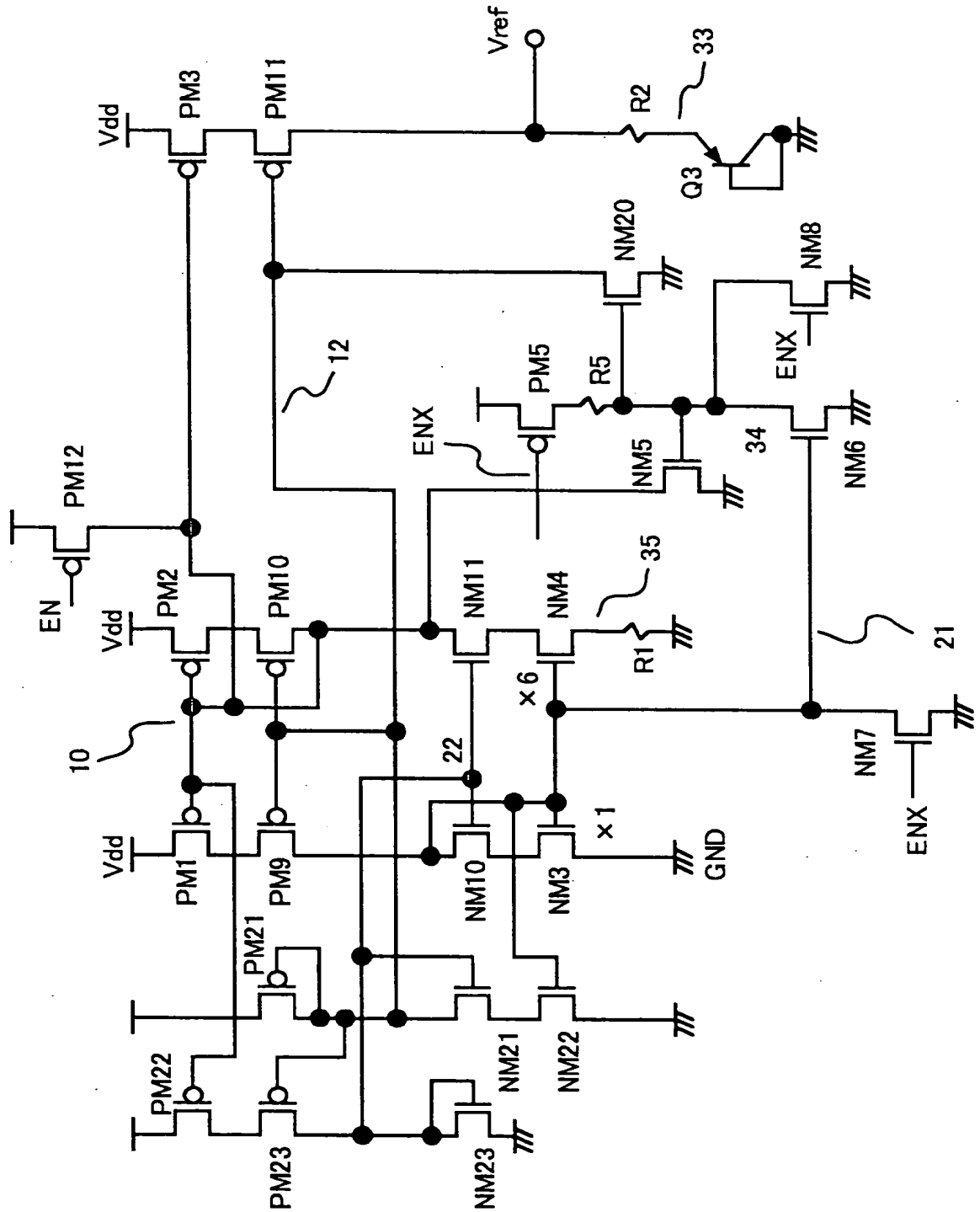




FIG.17

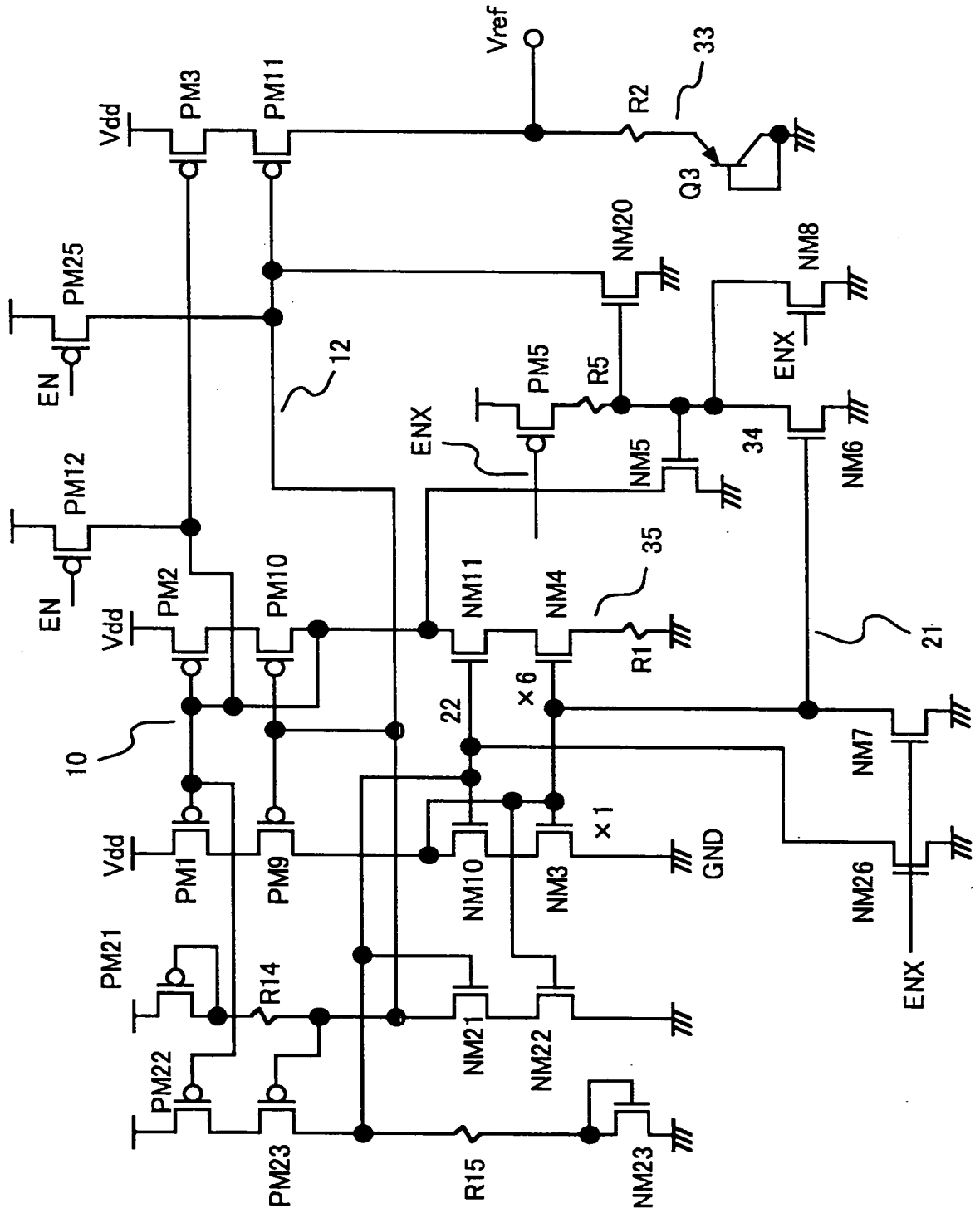
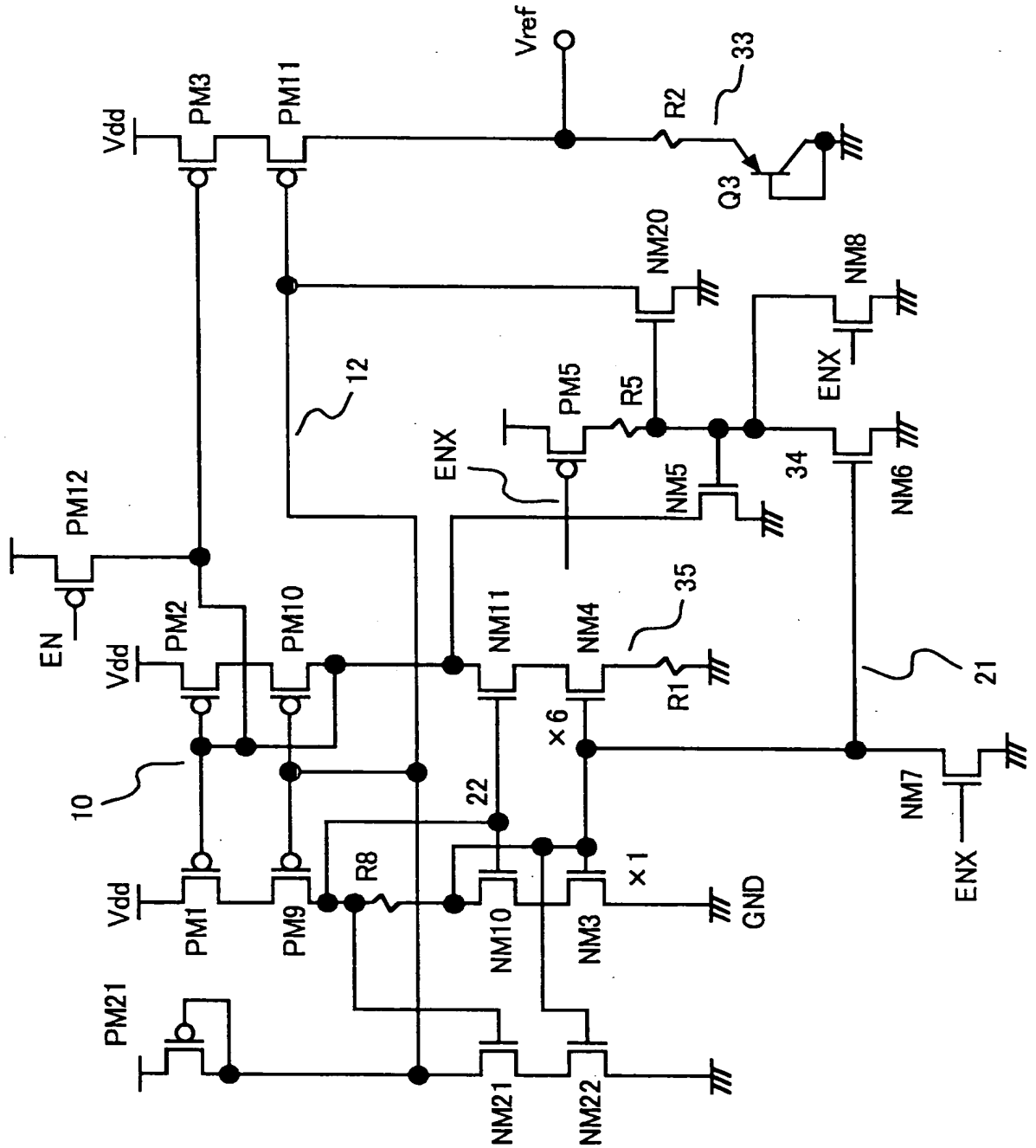


FIG.18



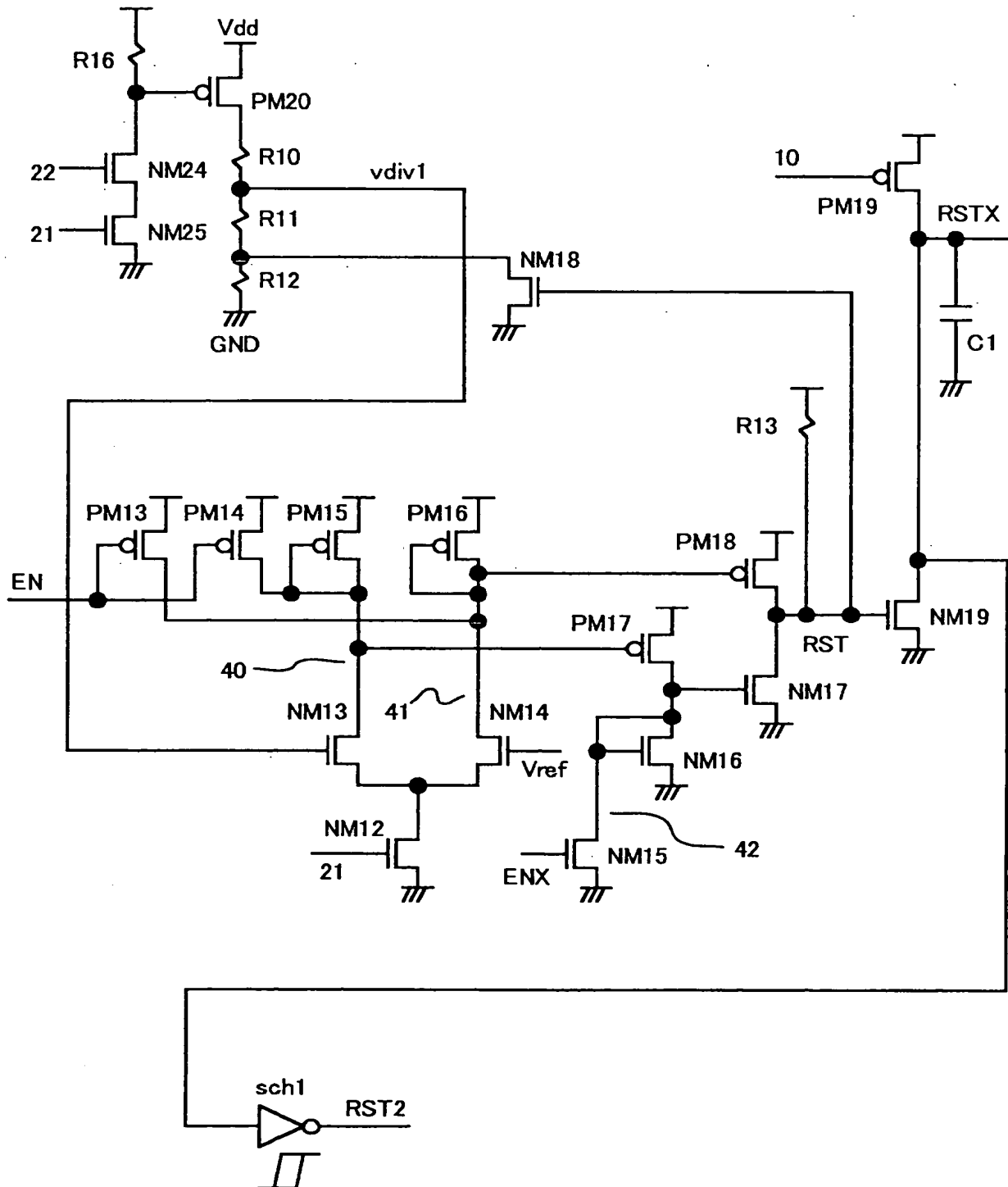


FIG.20

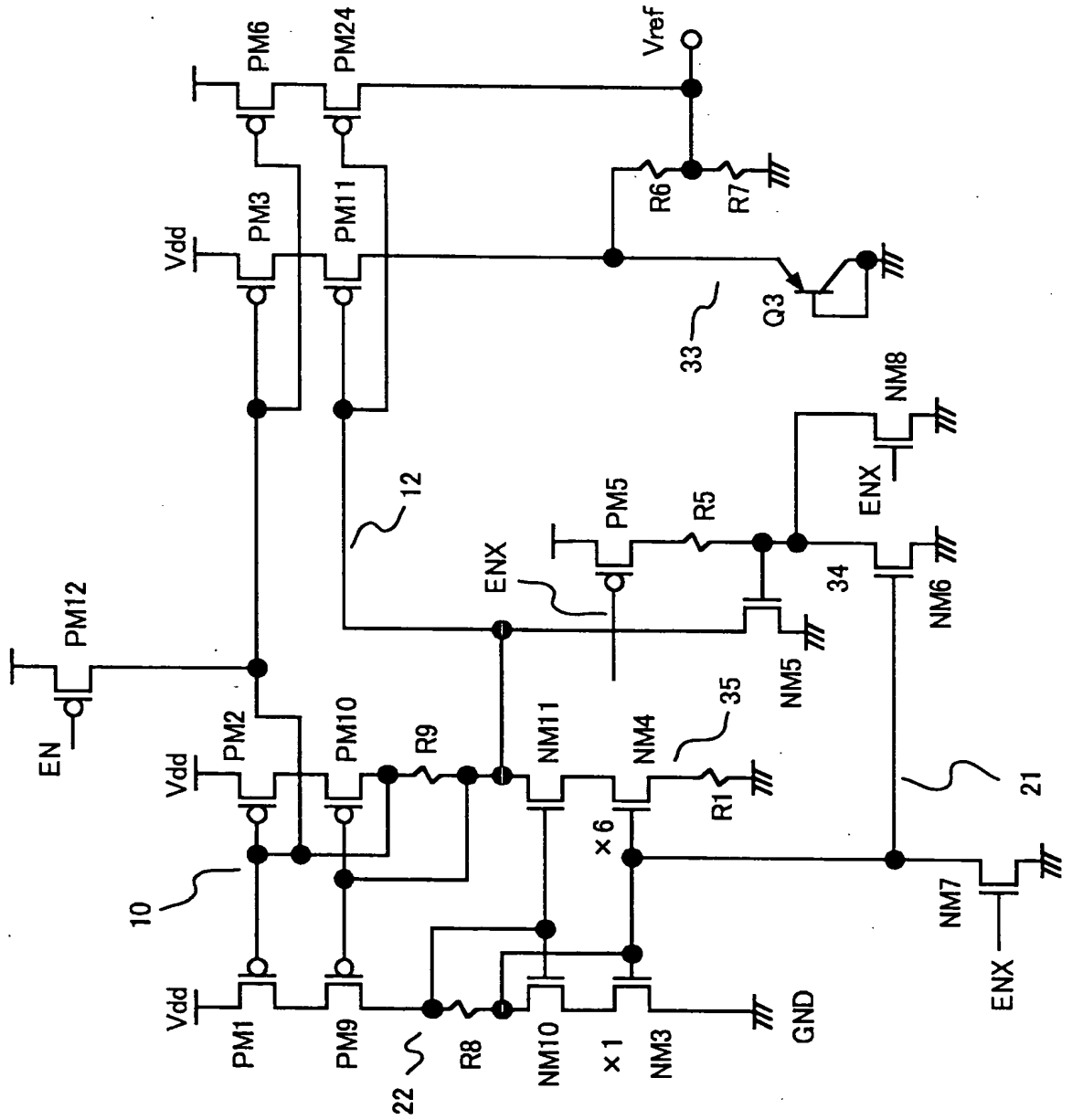


FIG.21

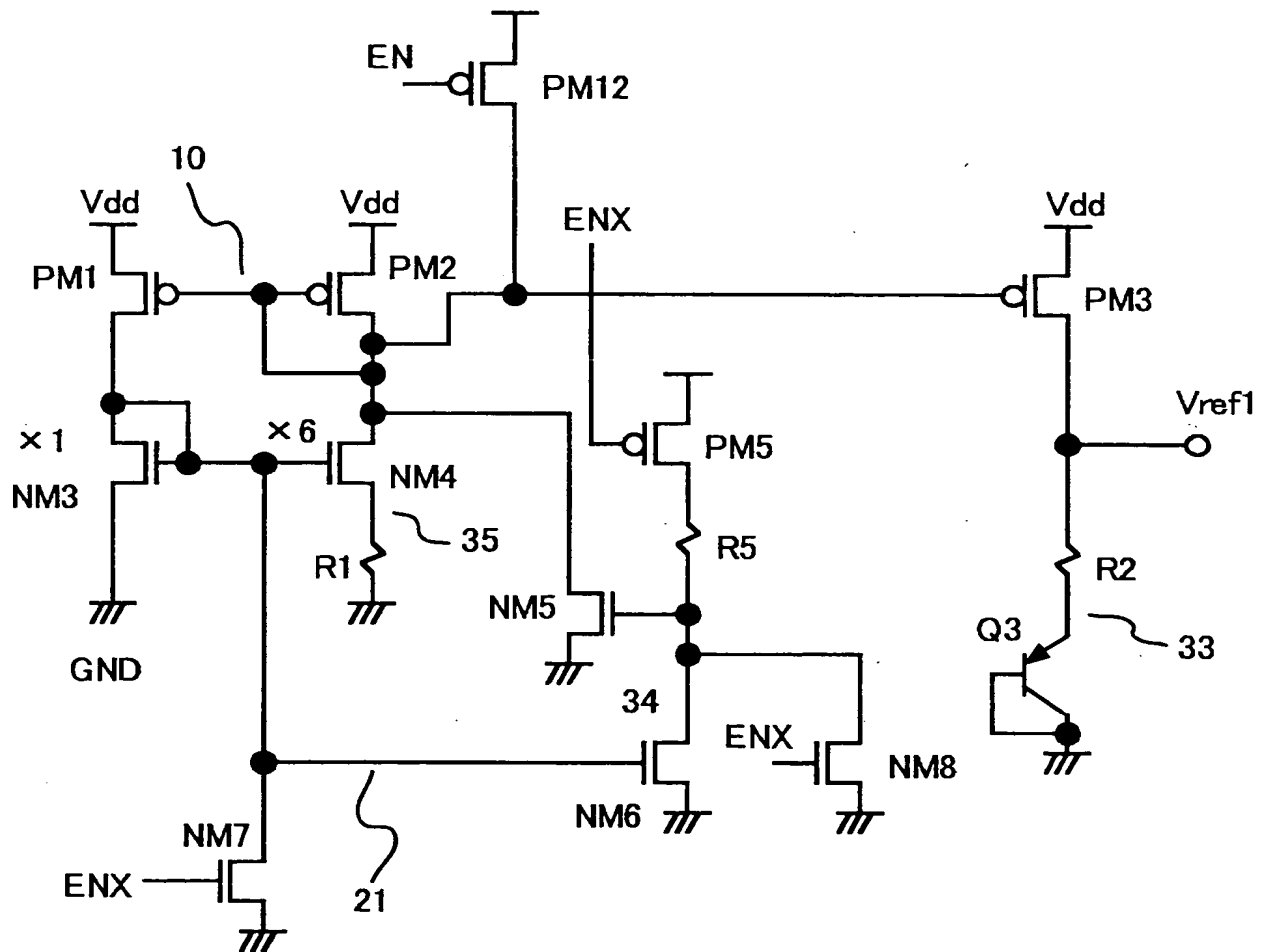
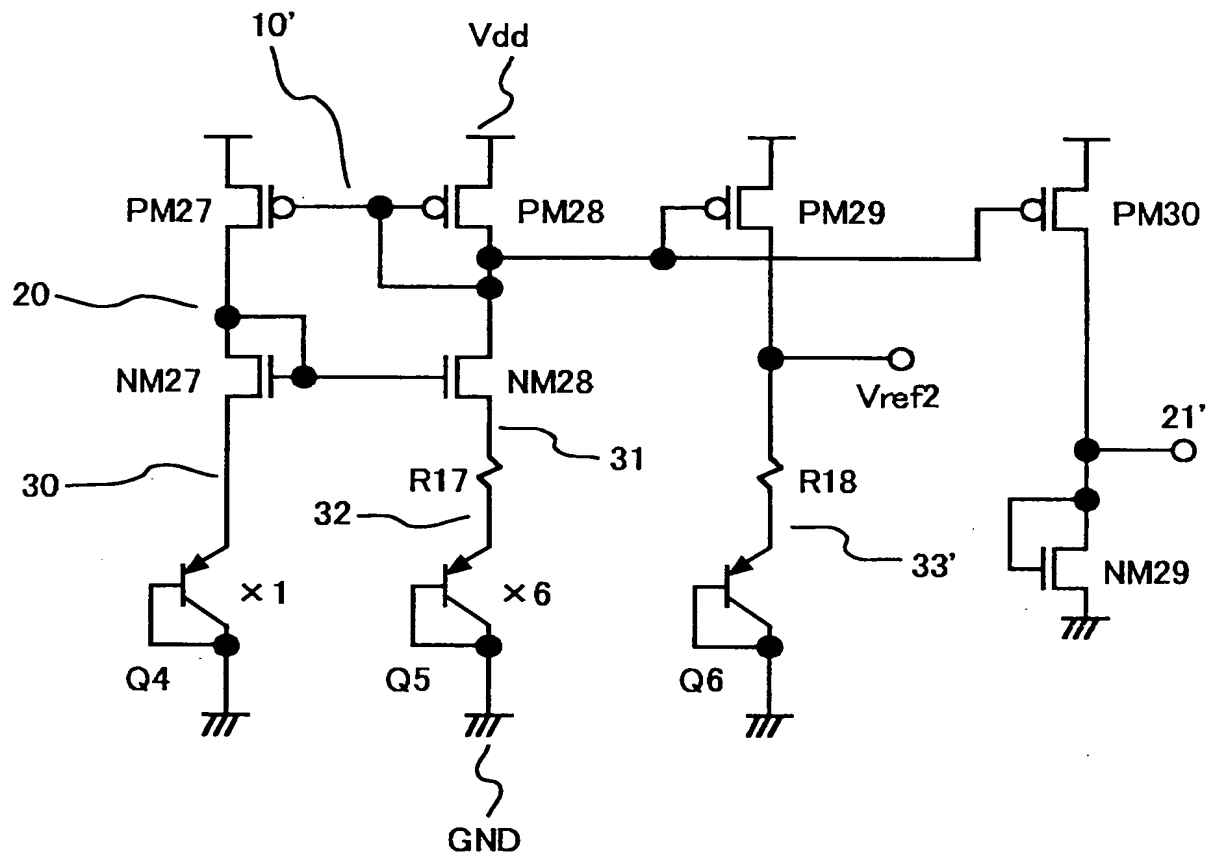


FIG.22



The diagram illustrates a multi-channel differential amplifier circuit, likely for a sensor interface, featuring two main processing channels (40 and 40') and associated control logic.

**Channel 40 (Top):**

- Input Stage:** A differential pair of NMOS transistors (NM13, NM14) with PMOS load devices (PM13, PM14, PM15, PM16). The gates of PM13, PM14, and PM15 are connected to the EN signal. The gates of PM15 and PM16 are connected to the ENX signal. The sources of NM13 and NM14 are connected to a common source node (41), which is biased by a current source NM12 connected to GND. The gates of NM13 and NM14 are connected to a bias network consisting of resistors R20, R21, R11, and R12, which is also connected to Vdd and GND. The output of this stage is taken from the drain of NM14, which is connected to a PMOS transistor (PM17) and a resistor R13.
- Output Stage:** A second differential pair of NMOS transistors (NM16, NM17) with PMOS load devices (PM17, PM18). The gates of PM17 and PM18 are connected to the EN signal. The gates of NM16 and NM17 are connected to the ENX signal. The sources of NM16 and NM17 are connected to a common source node (42), which is biased by a current source NM15 connected to GND. The gates of NM16 and NM17 are connected to a bias network consisting of resistors R19, R20, R21, R11, and R12, which is also connected to Vdd and GND. The output of this stage is taken from the drain of NM17, which is connected to a PMOS transistor (PM19) and a resistor R13.

**Channel 40' (Bottom):**

- Input Stage:** A differential pair of NMOS transistors (NM30, NM31) with PMOS load devices (PM32, PM33, PM34, PM35). The gates of PM32, PM33, and PM34 are connected to the EN signal. The gates of PM34 and PM35 are connected to the ENX signal. The sources of NM30 and NM31 are connected to a common source node (41'), which is biased by a current source NM32 connected to GND. The gates of NM30 and NM31 are connected to a bias network consisting of resistors R20, R21, R11, and R12, which is also connected to Vdd and GND. The output of this stage is taken from the drain of NM31, which is connected to a PMOS transistor (PM36) and a resistor R13.
- Output Stage:** A second differential pair of NMOS transistors (NM33, NM34) with PMOS load devices (PM36, PM37). The gates of PM36 and PM37 are connected to the EN signal. The gates of NM33 and NM34 are connected to the ENX signal. The sources of NM33 and NM34 are connected to a common source node (42'), which is biased by a current source NM33 connected to GND. The gates of NM33 and NM34 are connected to a bias network consisting of resistors R19, R20, R21, R11, and R12, which is also connected to Vdd and GND. The output of this stage is taken from the drain of NM34, which is connected to a PMOS transistor (PM19) and a resistor R13.

**Control Logic:**

- ENX:** A global enable signal that controls the gates of PMOS transistors PM20, PM31, PM15, PM16, PM17, PM18, PM34, PM35, PM36, and PM37.
- EN:** A global enable signal that controls the gates of PMOS transistors PM13, PM14, PM32, PM33, and PM34.
- RST:** A reset signal that controls the gates of NMOS transistors NM17 and NM35.
- RST2:** A reset signal that controls the gates of NMOS transistors NM17 and NM35.
- sch1:** A Schmitt trigger circuit that controls the gates of NMOS transistors NM17 and NM35.

FIG.24

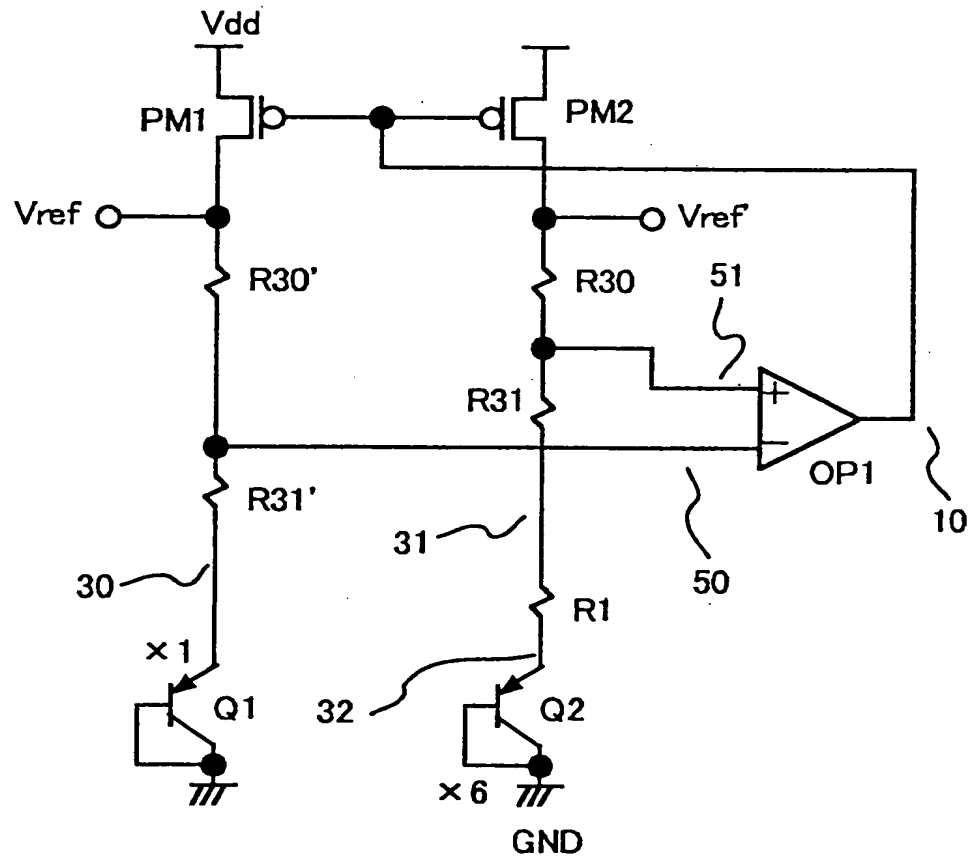




FIG. 25

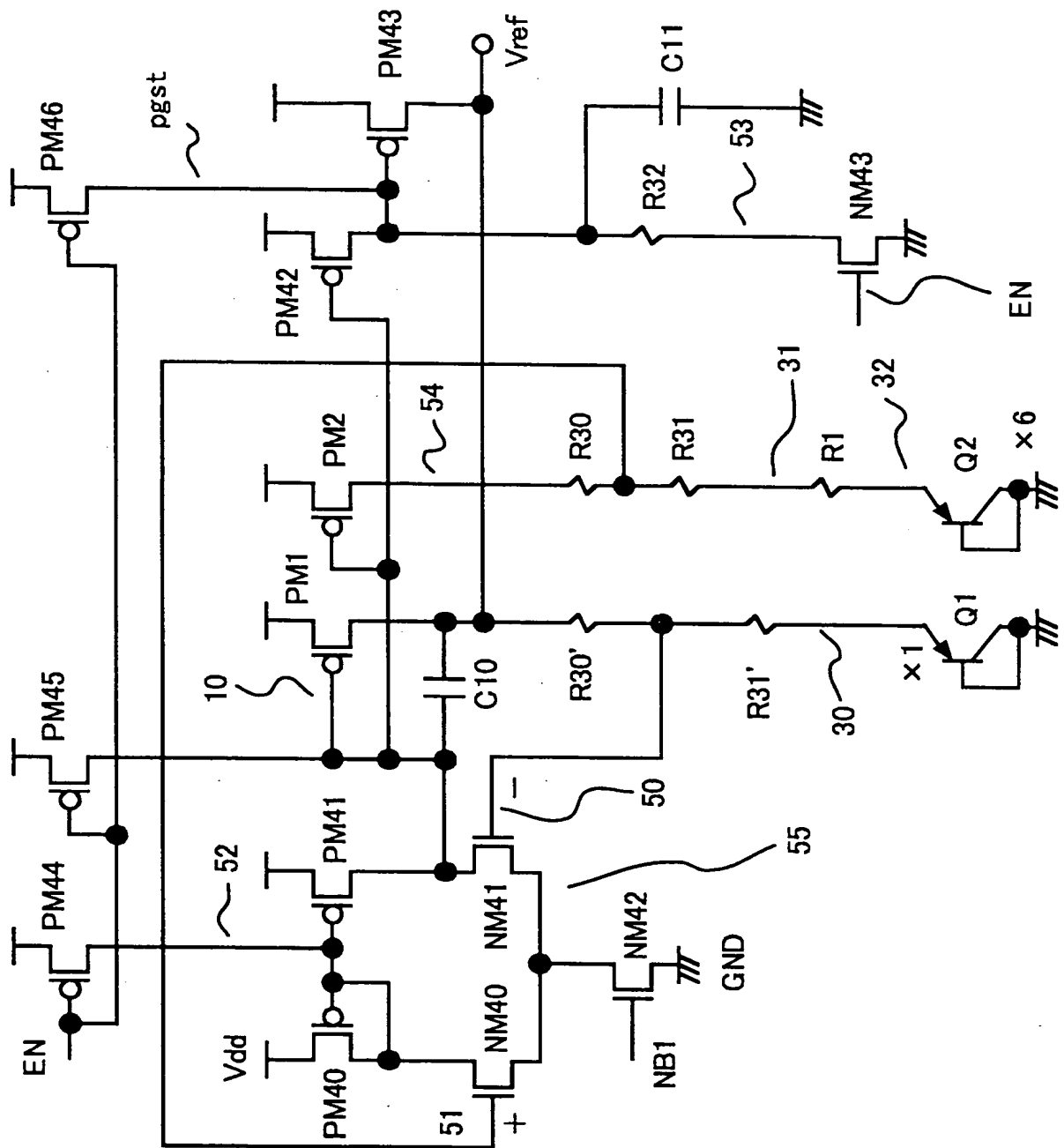
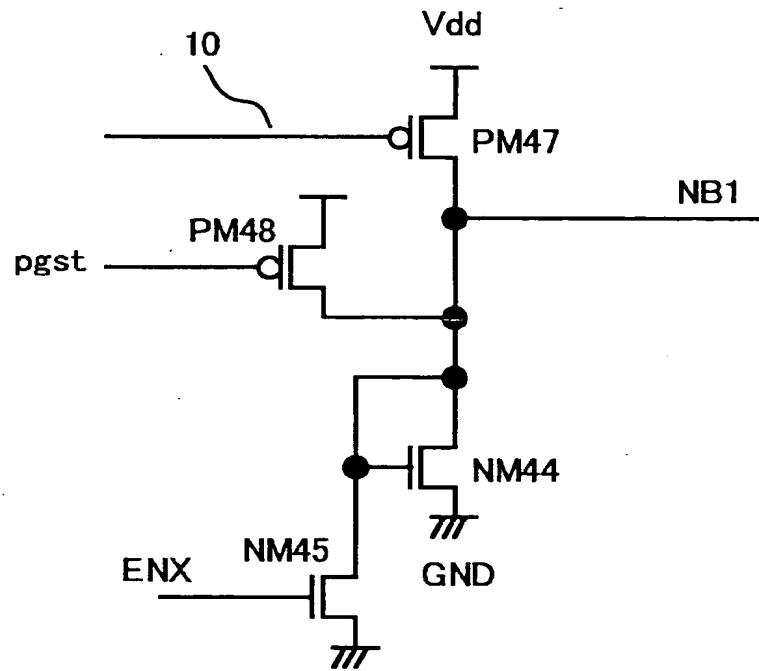
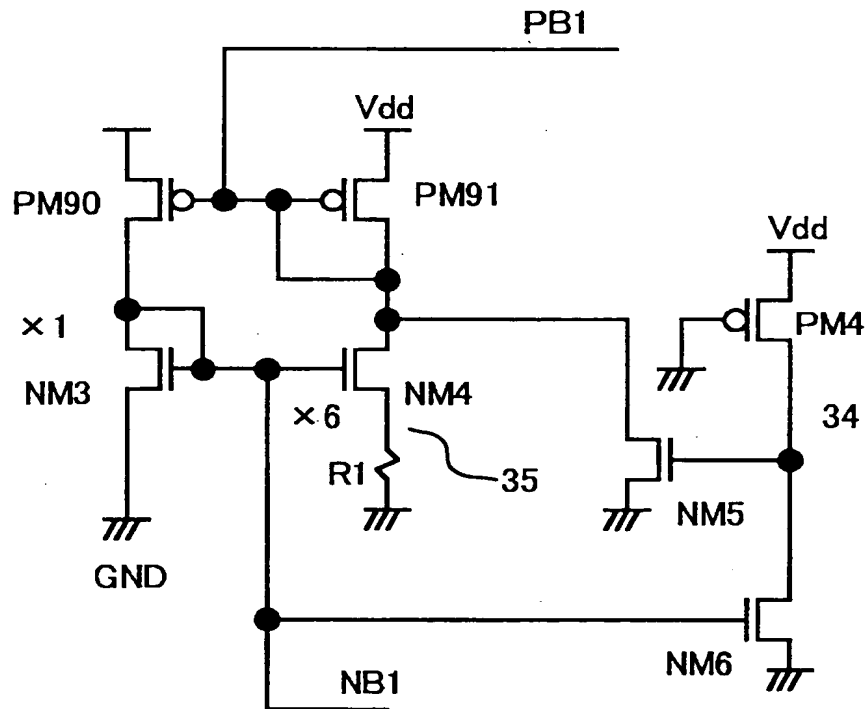


FIG.26



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FIG.27



**FIG. 28**

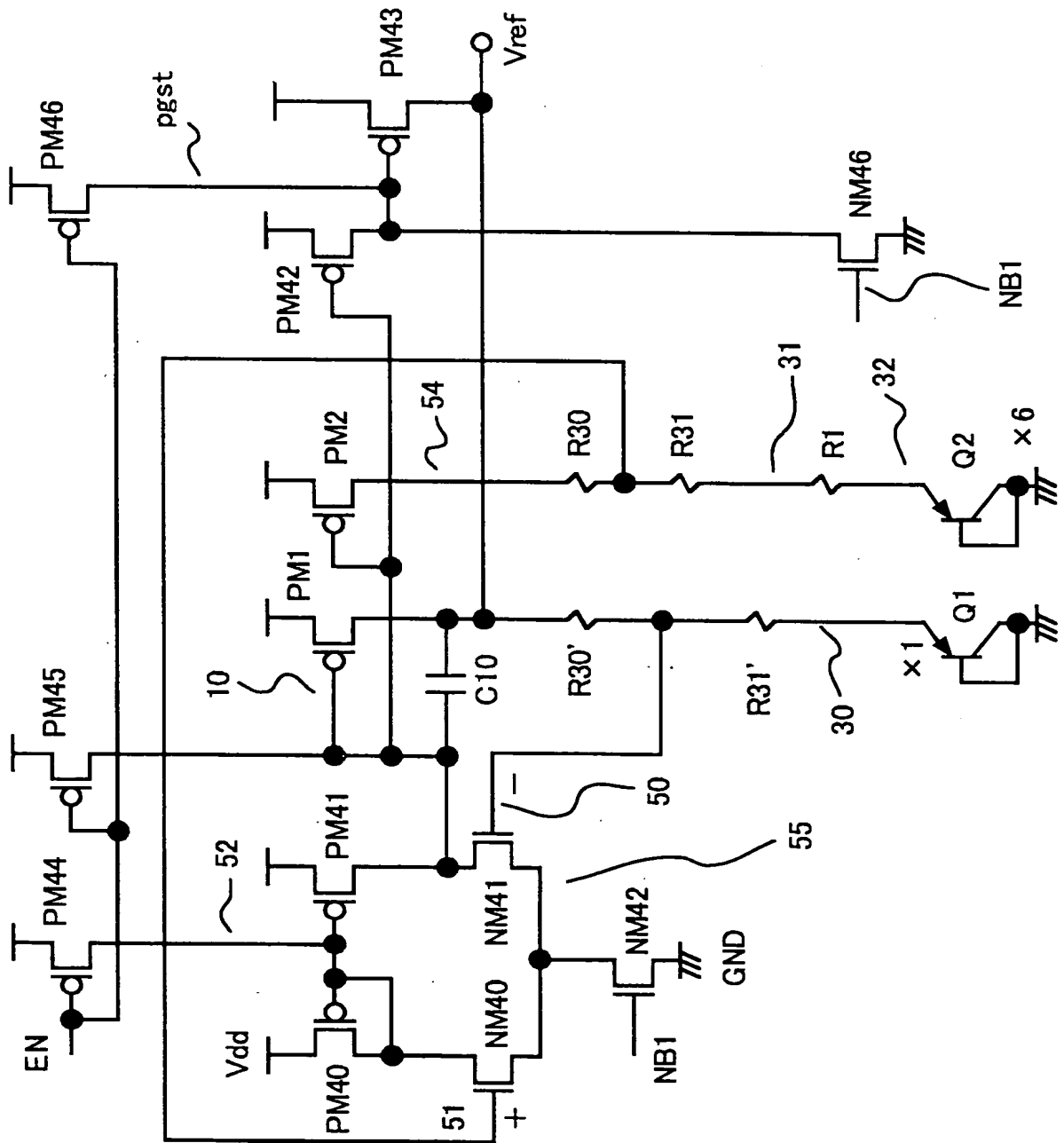


FIG.29

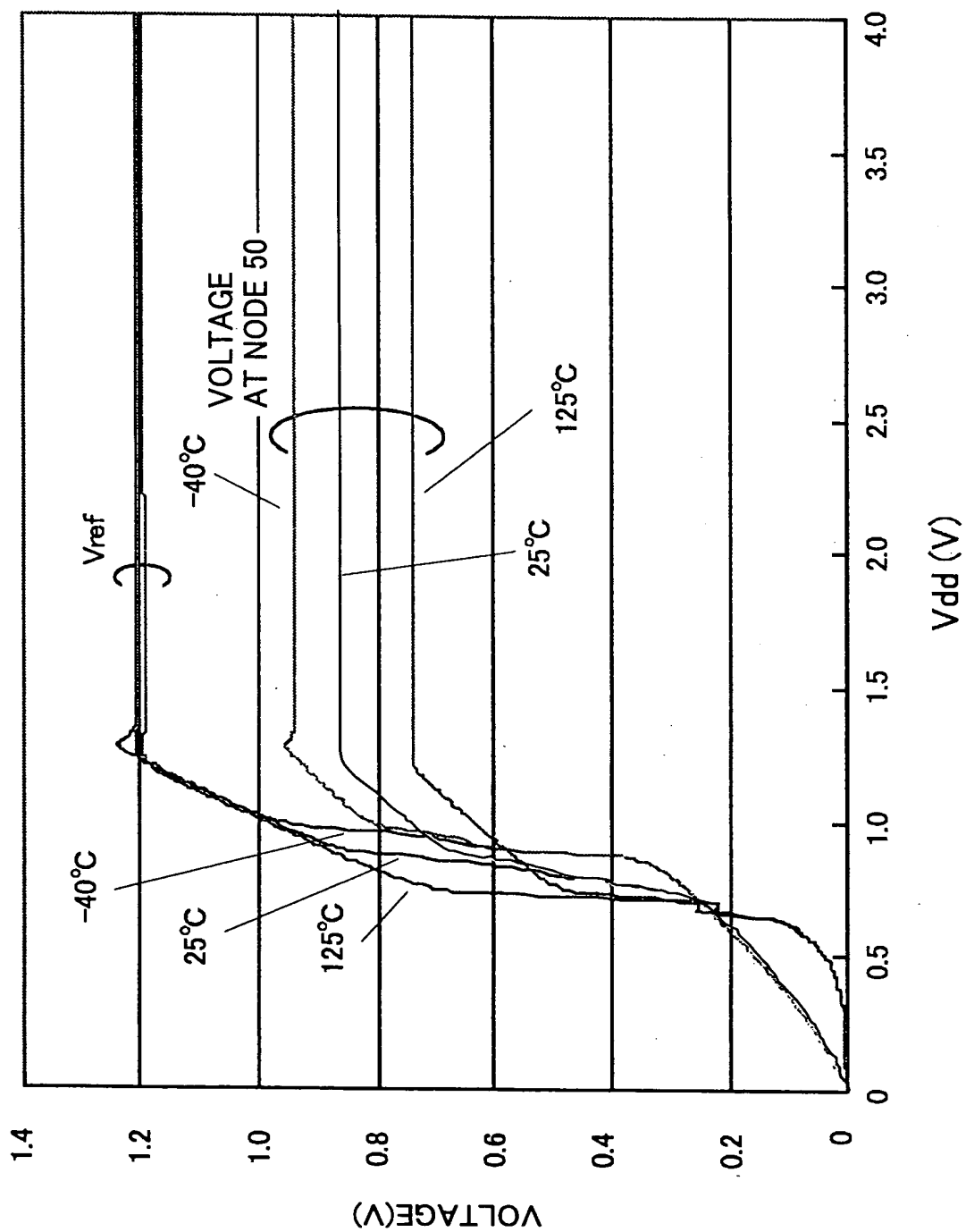
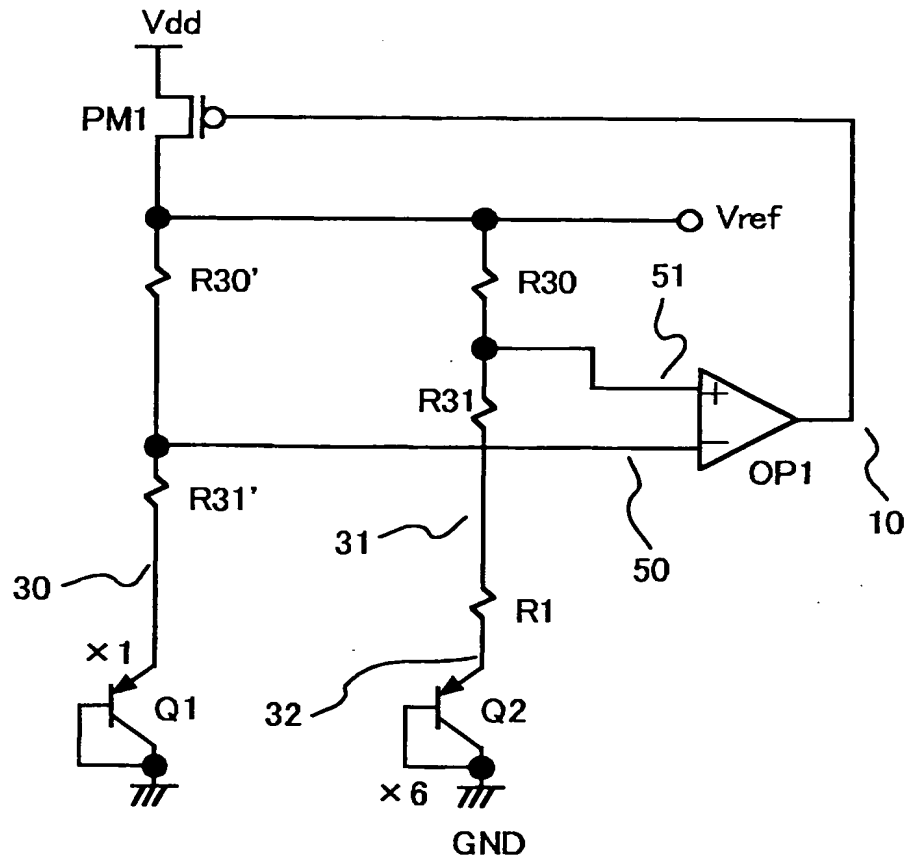
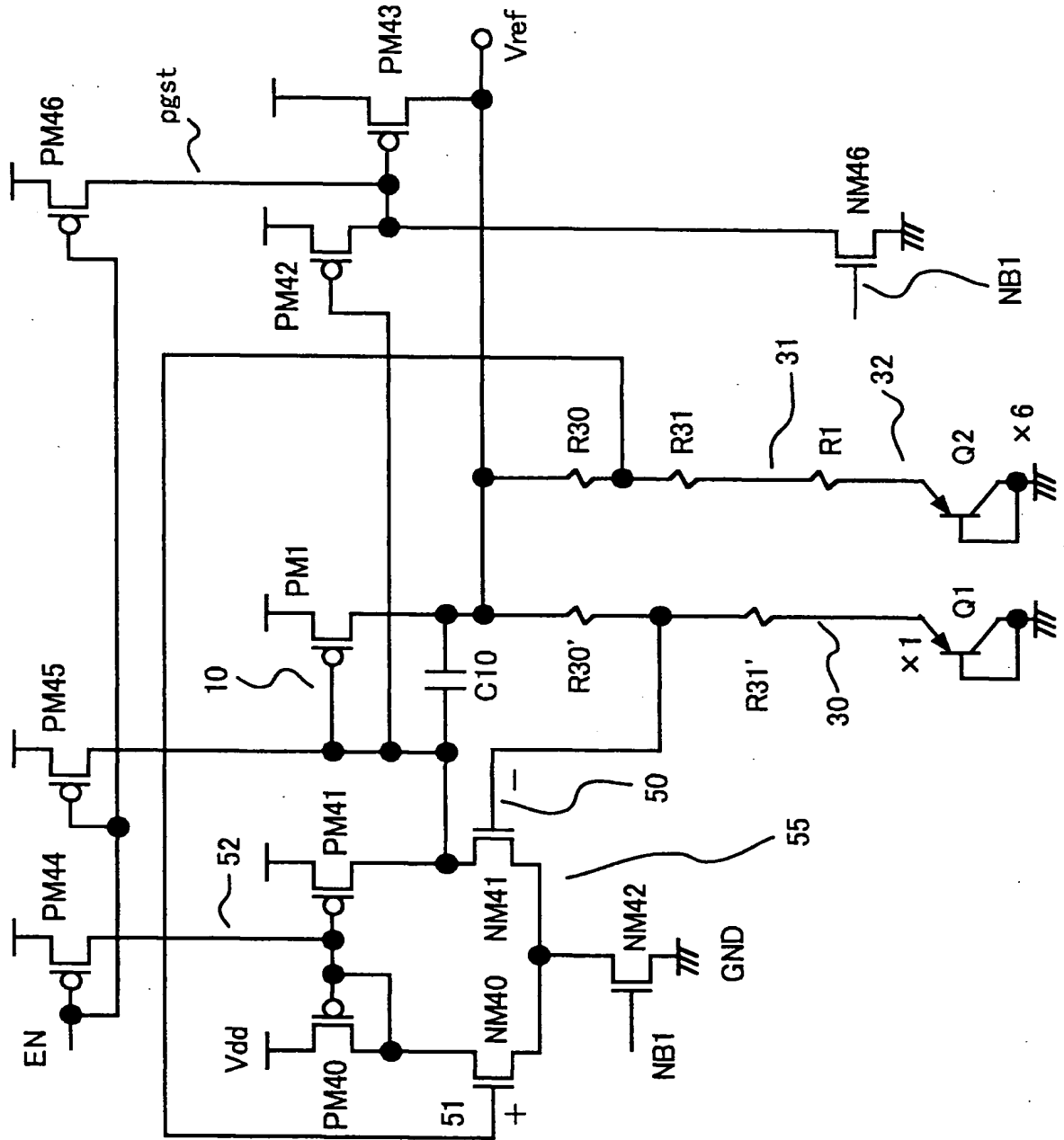


FIG.30

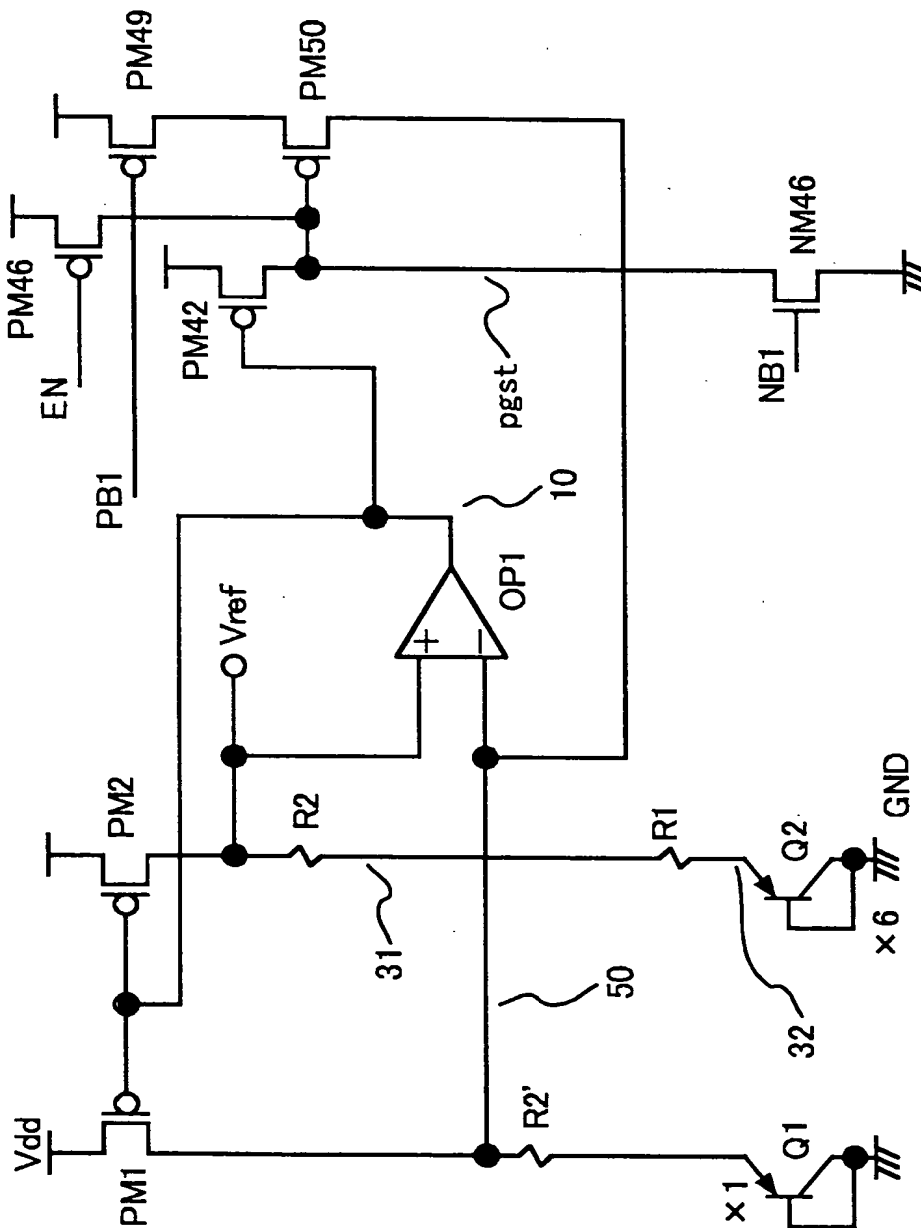


**FIG. 31**



Title: SEMICONDUCTOR INTEGRATED  
CIRCUIT  
Inventor: TACHIBANA, et al.  
Appln. No.: Unknown  
Docket No.: 100353-00185

**FIG. 32**





Title: SEMICONDUCTOR INTEGRATED  
CIRCUIT  
Inventor: TACHIBANA, et al.  
Appln. No.: Unknown  
Docket No.: 100353-00185

**FIG. 33**

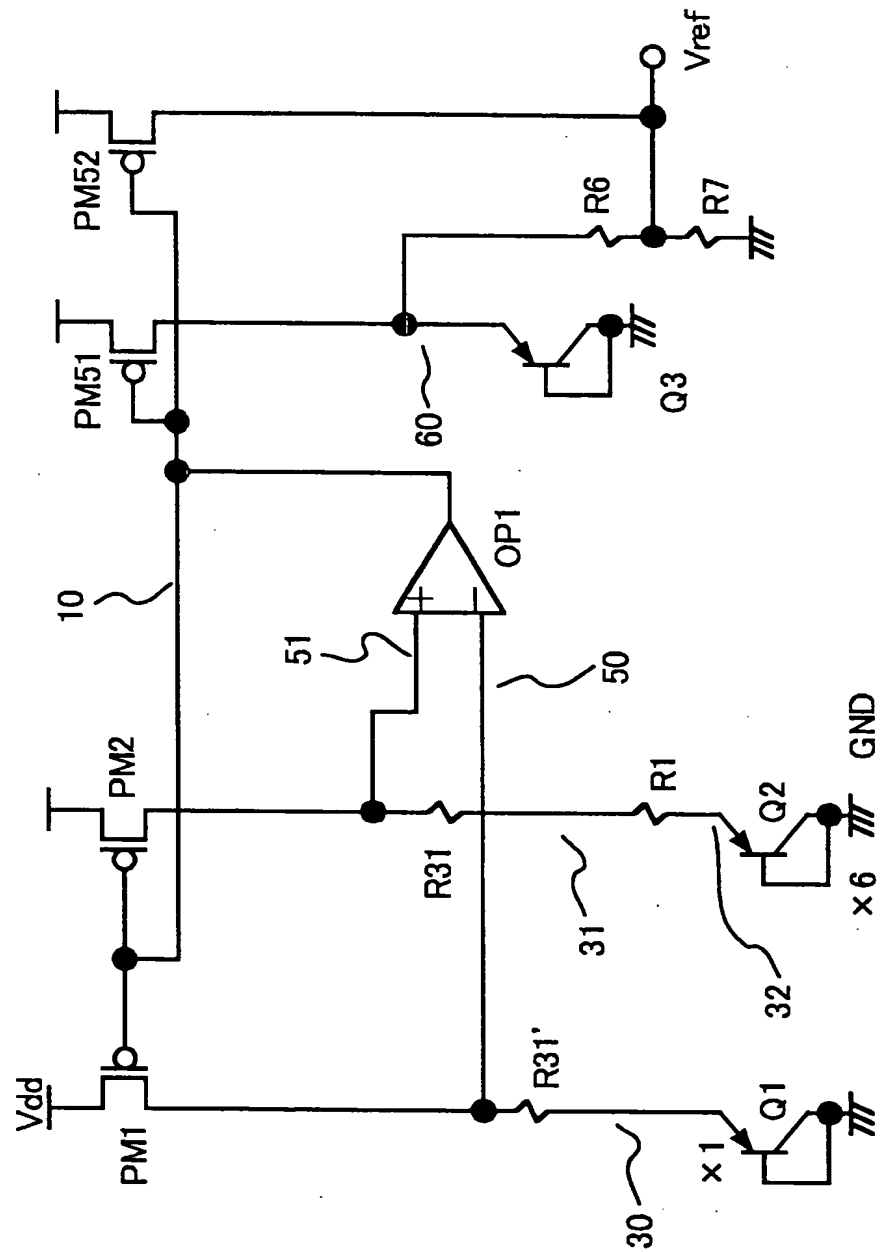


FIG.34

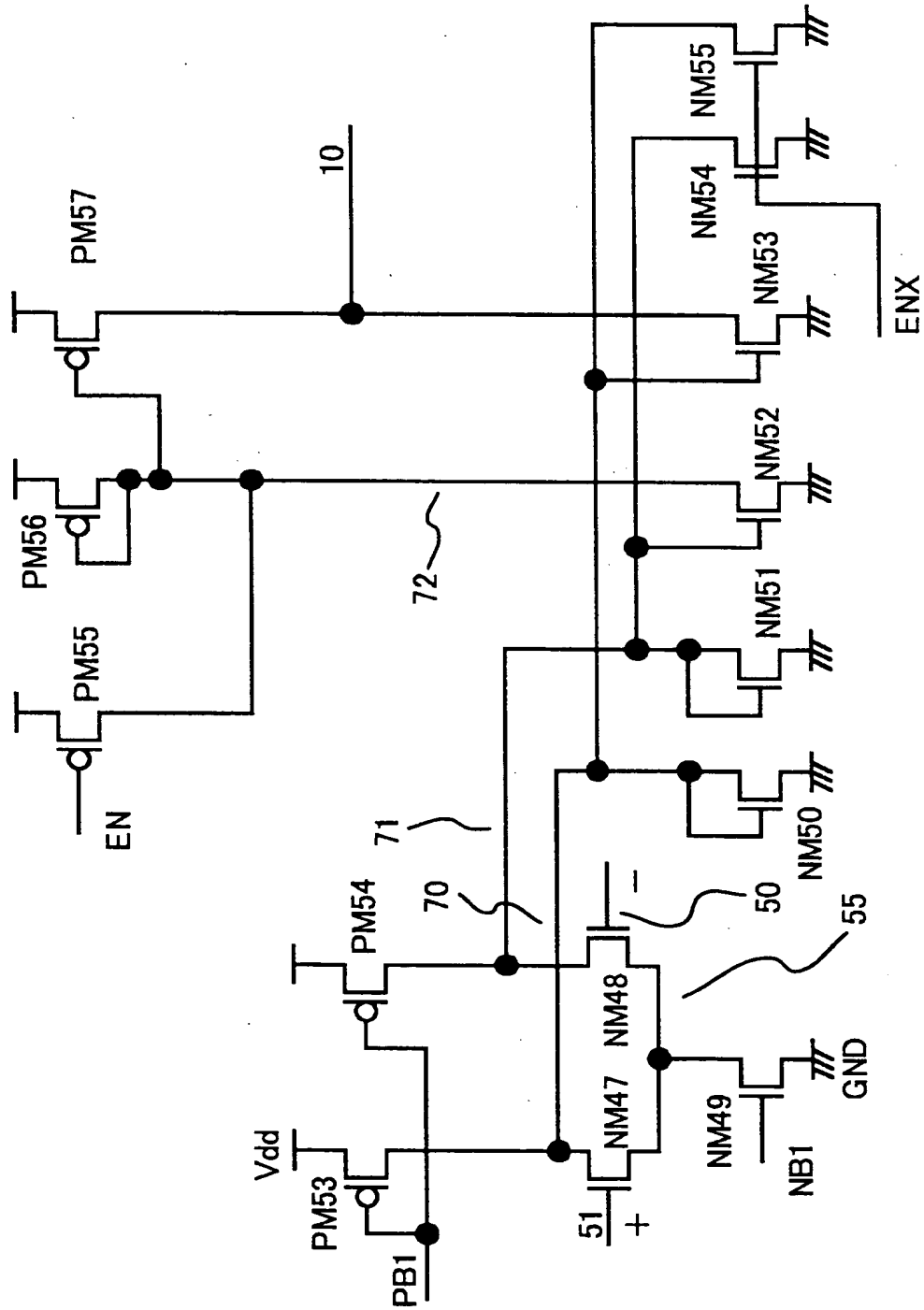
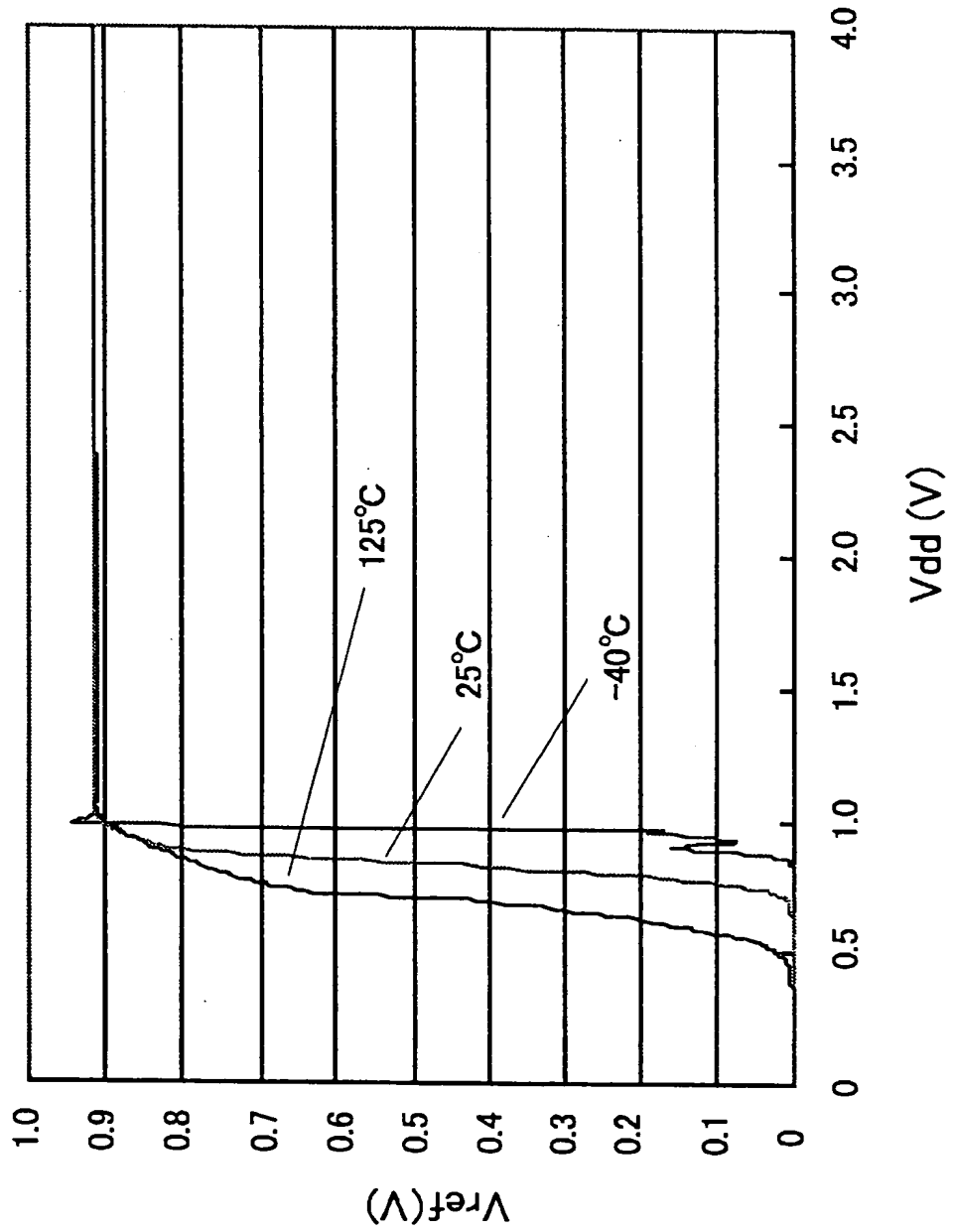


FIG.35



Title: SEMICONDUCTOR INTEGRATED  
CIRCUIT  
Inventor: TACHIBANA, et al.  
Appln. No.: Unknown  
Docket No.: 100353-00185

**FIG. 36**

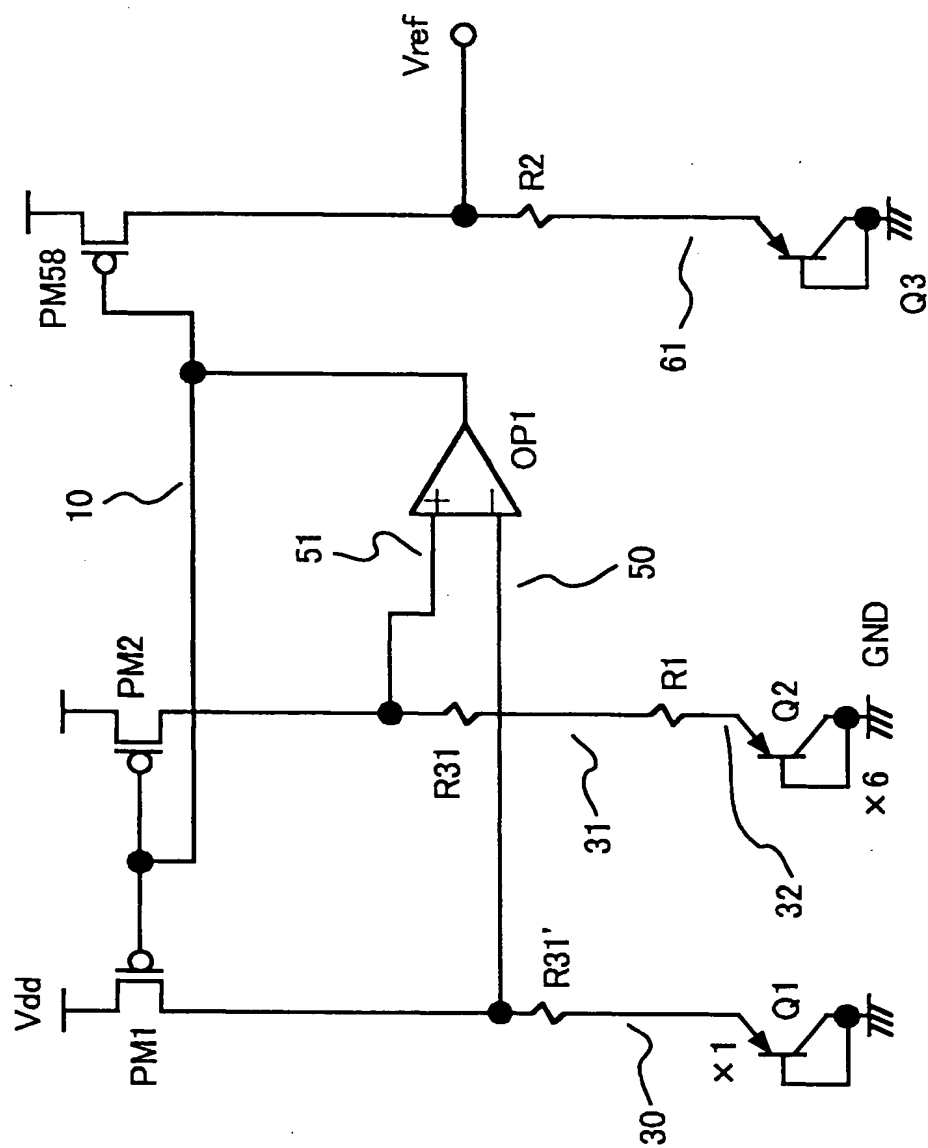


FIG.37

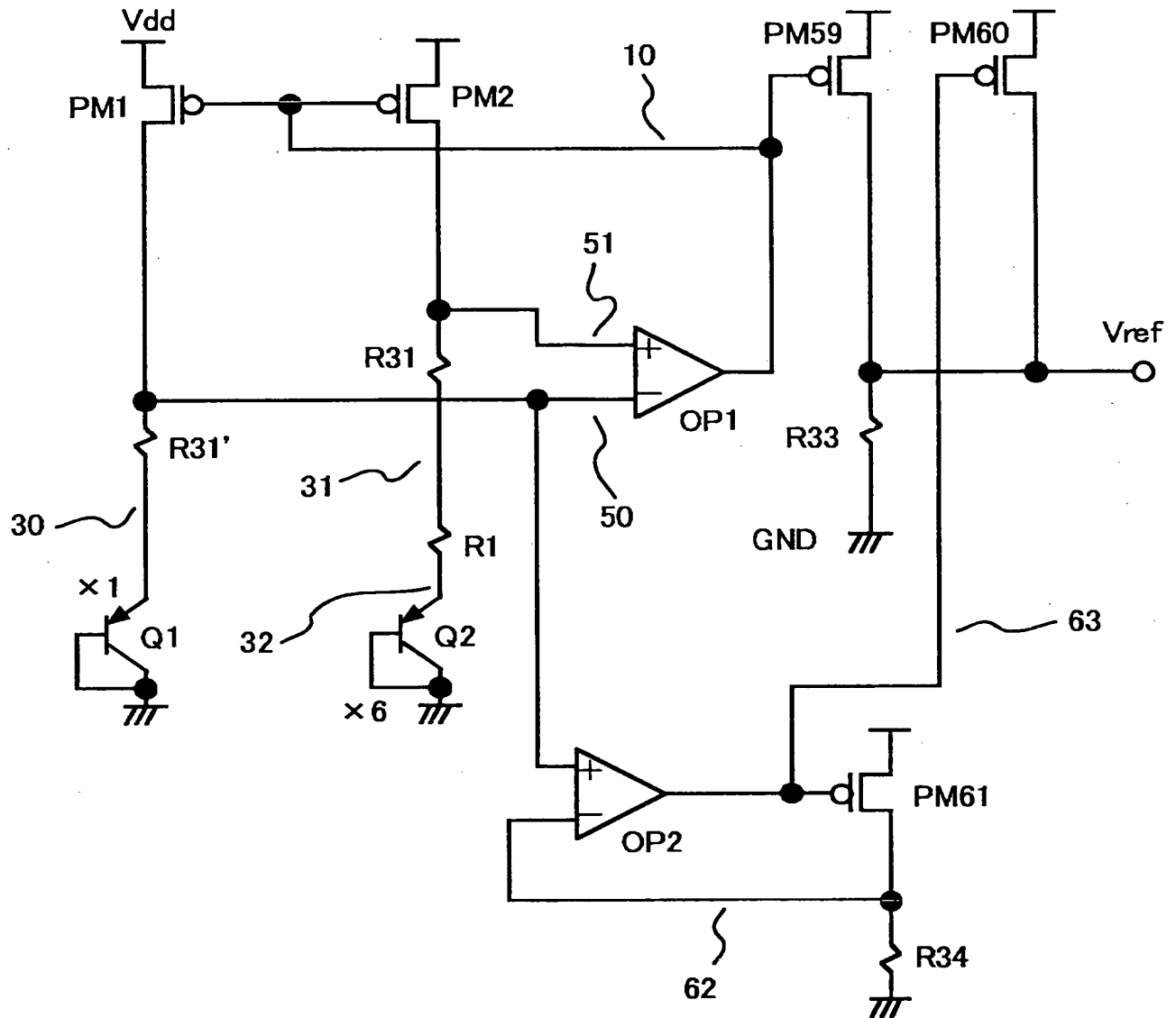


FIG.38

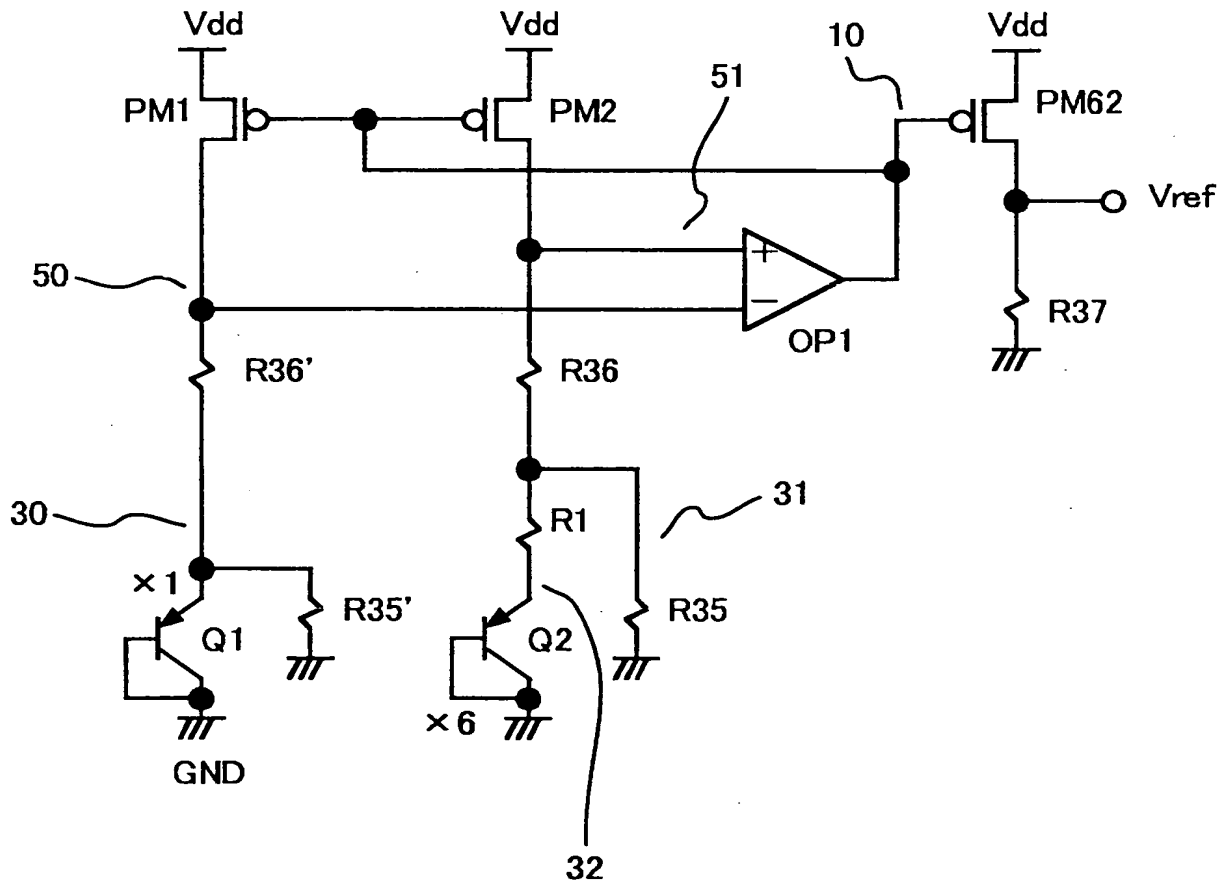
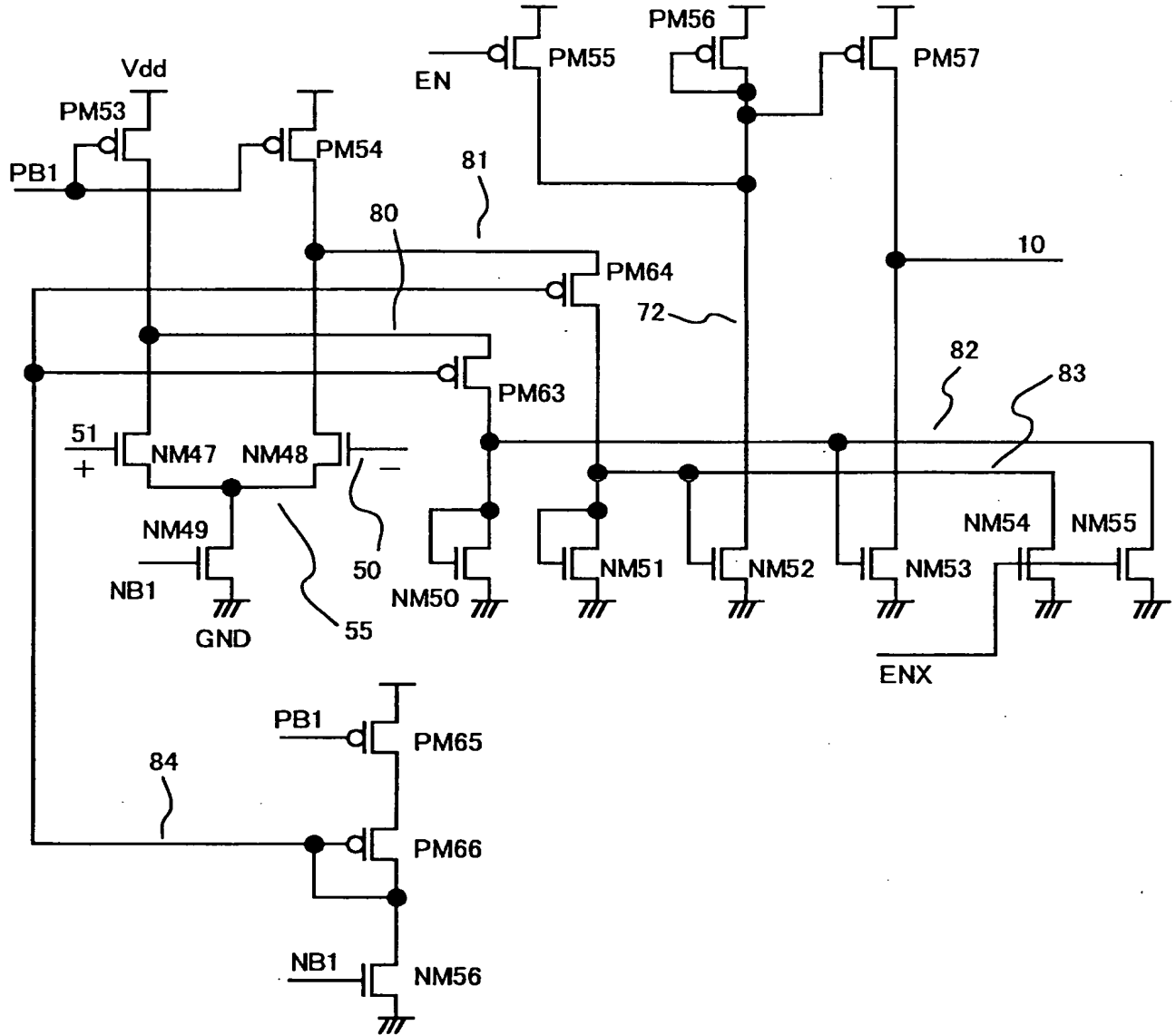


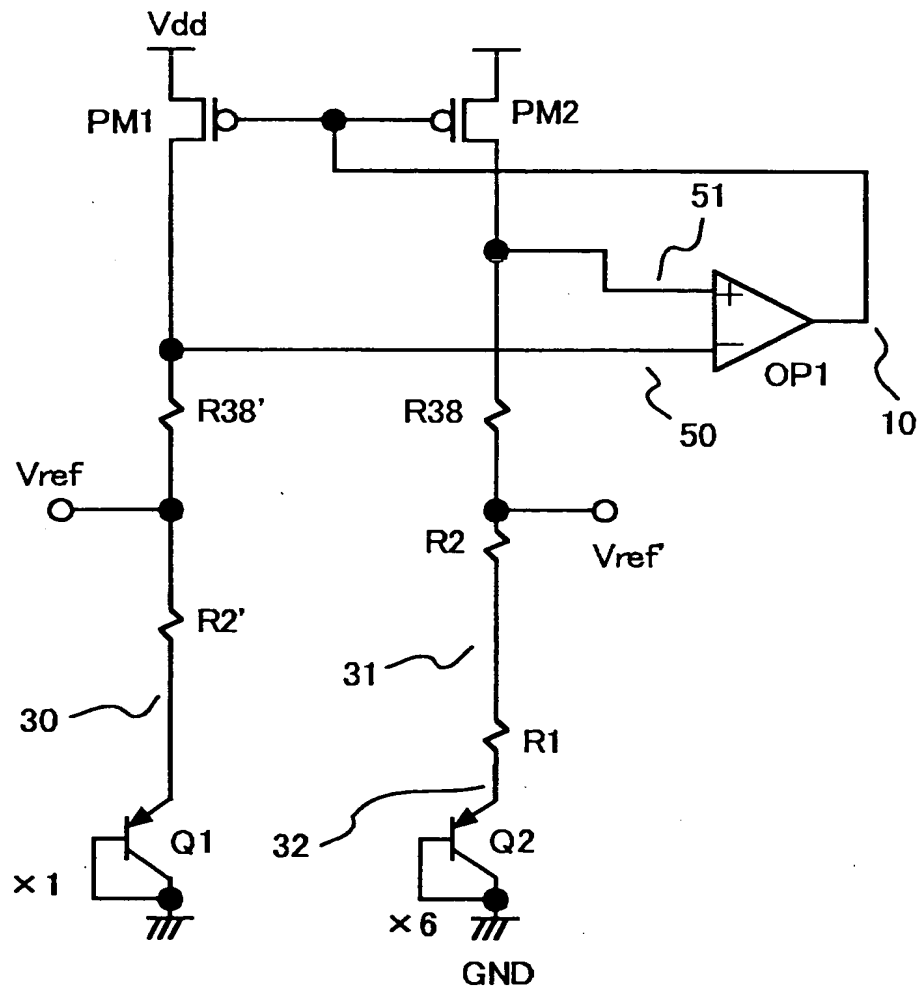
FIG.39



Docket No.: 100353-00185



FIG.41



The diagram illustrates a multi-bit DAC circuit. The top section features a feedback loop containing an operational amplifier (OP3) and a resistor network (R1, R30, R31, R30', R31'). The input to the DAC is a digital signal PB1, which is connected to a PMOS transistor (PM70) and a network of resistors (R30', R31'). The output of the DAC is a current, which is converted to a voltage by a resistor (R1) and then amplified by the OP3. The feedback loop is completed by a resistor (R30) and a PMOS transistor (PM71). The bottom section shows a multi-bit DAC core with PMOS (PM72, PM73, PM74, PM75, PM76, PM77) and NMOS (NM72, NM73, NM74, NM75, NM76) transistors, and a current source (NB1). The output of the DAC core is a current, which is converted to a voltage by a resistor (R1) and then amplified by the OP3. The feedback loop is completed by a resistor (R30) and a PMOS transistor (PM71).

FIG.43

